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A System-Verilog Verification Environment for the CIC Data Concentrator ASIC of the CMS Outer Tracker Phase II Upgrades

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High data rate requirements of the CMS Outer Tracker front-end electronics in the High-Luminosity LHC and the optimum utilization of the optical link bandwidth necessitate the development of a data aggregator ASIC; namely Concentrator IC (CIC).
To facilitate the RTL code development and to allow functional verification of the CIC ASIC in the context of the entire readout chain, a simulation framework was built incorporating all front-end ASICs; Macro Pixel ASIC (MPA) and Short Strip ASIC (SSA) for Pixel-Strip (PS) modules and CMS Binary Chip (CBC) for Strip-Strip (2S) modules.

Summary

The foreseen Phase II upgrades at the LHC present very challenging requirements for the front-end readout electronics of the CMS Outer Tracker detector. High data rates in combination with the employment of a novel technique for rejecting locally low transverse momentum particles as well as the strict low power consumption constraints require the implementation of an optimized readout architecture and specific interconnect synchronization schemes for its components. To facilitate the design of the complete front-end readout chain and the development of the ASIC components a system-level simulation framework was developed based on the industry standard SystemVerilog language and the Universal Verification Methodology (UVM) platform. This work focuses its scope on the development work and design verification of the Concentrator IC (CIC) ASIC.
The CIC is a 65 nm CMOS technology ASIC that receives high frequency (320MHz) digital data streams from 8 Front-end ASICs via a total of 48 differential lines and transmits them through 7 differential lines running at 320 MHz or 640MHz frequency as required by the detector module occupancy. The amount of data at the input is 15.36 Gb/s while the output data is up to 4.48 Gb/s at 640 MHz data rate. The CIC needs to interface with two different types of ASICs; namely the Macro Pixel ASIC (MPA) for the Pixel-Strip (PS) modules and the CMS Binary Chip (CBC) for Strip-Strip (2S) modules.
The verification environment is able to perform clock-cycle accurate behavioral simulations using either a custom random hit generator or Monte-Carlo generated hits from Physics simulations. Random hit generation can be tailored according to the front-end ASIC: MPA or CBC. The test environment components are implemented at the Transaction Level Modelling (TLM) level. At this level of abstraction, higher than the RTL, channels hide the complexity of the protocols and the communication is implemented in the form of function calls instead of signals. The details of the communication among components is decoupled from the details of their implementation. The communication between verification components, reference model and scoreboards is based on transaction objects. This approach allows to achieve a modular implementation easy to extend and reuse while accelerating the simulation time. Several scoreboards allow to perform conformity checks between predicted and actual ASIC component outputs. This contribution will present in detail the simulation framework focusing on the in-system verification work performed for the CIC ASIC during its prototype development phase.

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