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Algorithms for Threshold Dispersion Minimization of the CHIPIX65 Asynchronous Front-End

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This work discusses four different algorithms for the minimization of threshold dispersion in multichannel readout circuits for pixel detectors. These algorithms, which are based on different methods (e.g. charge scans, threshold scans, etc) and differs in terms of performance and computation time, have been tested on the asynchronous front-end integrated in the CHIPIX65_FE0, a readout ASIC prototype designed in a 65nm CMOS technology.

Summary

Extraordinarily high levels of radiation and particle rates will be attained in the high-luminosity upgrades of the Large Hadron Collider experiments.
The instantaneous luminosity will be five times the nominal one, reaching 5*10^34 cm^(-2)s^(-1), while the expected level of radiation for the innermost layers of the tracking pixel detectors is 1 Grad in 10 years.
These harsh conditions will set tough requirements for the readout chips in that part of the CMS and ATLAS detectors.

The CERN RD53 collaboration was founded in 2013 to investigate new technologies and architectures for future readout chips.
The Italian Institute for Nuclear Physics (INFN), through the CHIPIX65 project, has been actively contributing to RD53, which served the purpose of testing design solutions by means of a small-scale demonstrator called CHIPIX65_FE0.

The purpose of this work is to describe four threshold tuning algorithms and to discuss their performance in terms of threshold dispersion and operation time.

The prototype developed by the CHIPIX65 project integrates a 64x64 pixel matrix, divided in two 32x64 sub-matrices with 50um pixel pitch.
This paper reports on threshold dispersion measurements on the sub-matrix integrating an asynchronous front-end composed of a charge sensitive amplifier followed
by a low-power, high-speed comparator combined with a 5-bit, dual edge time over threshold (TOT) counter.
Channel-to-channel threshold dispersion is addressed by means of an in-pixel threshold trimming DAC, based on a 4-bit binary weighted architecture, whose output range can be properly set by means of a DAC integrated in the matrix periphery.

The conference paper will report on the description of the algorithms together with the characterization results of the CHIPIX65 asynchronous front-end.

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