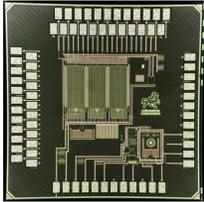


# An Ultra-Fast 10Gb/s 64b66b Data Serialiser Back-end in 65nm CMOS Technology

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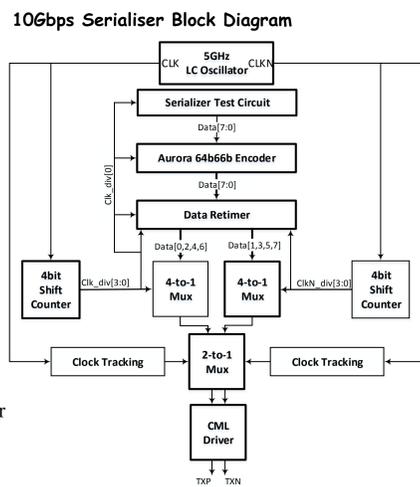


With future pixel ASICs trending towards mega-frame rate readout, the development of ultra-high-speed readout systems is increasingly important. Here we present an ultra-fast readout system developed to operate at 10Gb/s, and intended to surpass a more conventional highly-parallel LVDS bus approach. The system generates a 5GHz clock (LC Oscillator), scrambles and serialises the parallel input data in accordance with the Aurora 64b66b protocol, and transmits the data off-chip through a Current Mode Logic (CML) line-driver at 10Gb/s. A prototype is under evaluation having been fabricated in early 2018 on a 65nm Multi-Project Wafer. Serialiser ASIC ran at 10.302Gbps under test for 60 hours without a bit-error event.

## 10Gbps Serialiser ASIC

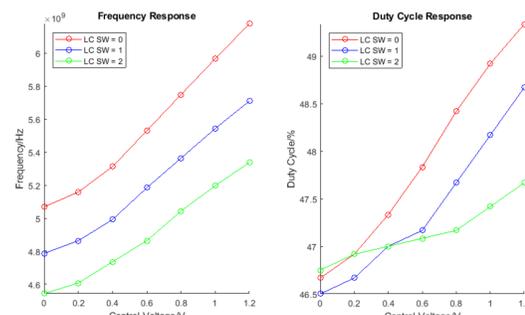
The 10Gbps Serialiser ASIC operates correctly at 10.302Gbps with Aurora 64b66b encoding enabled. From a long run test, the first bit error occurred in just over 60 hours. The 10Gbps Serialiser can be summarised in the diagram to the right with the following points:

- > A clean 5GHz clock is generated through a LC oscillator PLL.
- > 8 1.25GHz clocks with 100ps consecutive phase shift are generated through 2 4bit shift counters with both edges of the 5GHz clock.
- > Data is encoded in 8bit words every 800ps.
- > Encoded data is retimed into individual 300ps windows using all 8 1.25GHz clocks via multi-clock domain pipelining.
- > Retimed encoded data is split alternatively and multiplexed into 2 5Gbps bit-streams.
- > The 5Gbps bit-streams are then multiplexed into the final 10Gbps bit-stream with the phase-tracked 5GHz clock.
- > Finally the 10Gbps bit-stream is buffered and sent to the CML driver to be driven off chip.

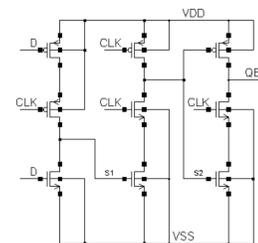


## LC Oscillator PLL

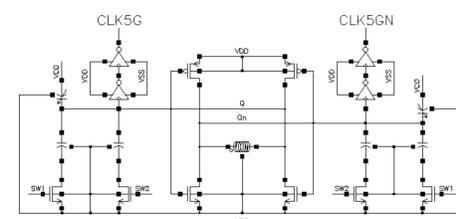
- LC oscillator was chosen for superior performance in jitter, duty cycle and stability.
- LC oscillator was attached to an analogue charge pump PLL architecture to meet the clock system requirements.
- Custom True Single Phase Clocking (TSPC) flip-flops were designed to operate at 5GHz plus and used in the PLL to divide the generated clock down. Also used in the Serialiser.
- Configurable capacitor damping allow additional tunability
- Duty cycle operates at 47% at 5GHz
- Frequency response is linear with a frequency range of 4.6 - 6.1GHz



## TSPC Flip-flop Schematic



## LC Oscillator Schematic



## Aurora 64b66b Encoding and ASIC Readout

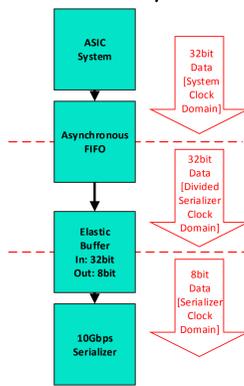
Aurora 64b66b protocol:

- Implemented due to being an efficient, robust and common protocol for high speed links.
- Scrambles the bit-stream to ensure it is DC-balanced for clean data-transmission.
- ASIC also transmits the following special Aurora packets:
  - Clock recovery packets – Allows the receiver and transmitter to operate on asynchronous clocks
  - End frame packets – Allows the bitstream to be split into packages.
  - Idle packets – When no data is available to be sent, idle packets are sent and then transparently stripped out at the receiver.

Readout system in development for future ASICs:

- Implements an asynchronous FIFO to allow the ASIC system and the 10Gbps Serialiser to operate asynchronously with varying frequencies.
- Utilises elastic buffer with multi clock cycle delays between the FIFO and the Serialiser to lower the minimum operating frequency of the FIFO.
- Serialiser automatically detects when the FIFO is empty through piped status flags and instead sends idle packets until data is available.

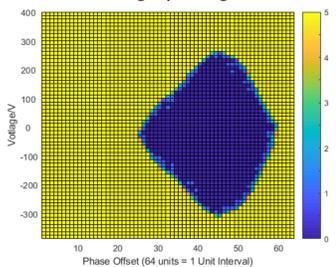
## ASIC Readout System



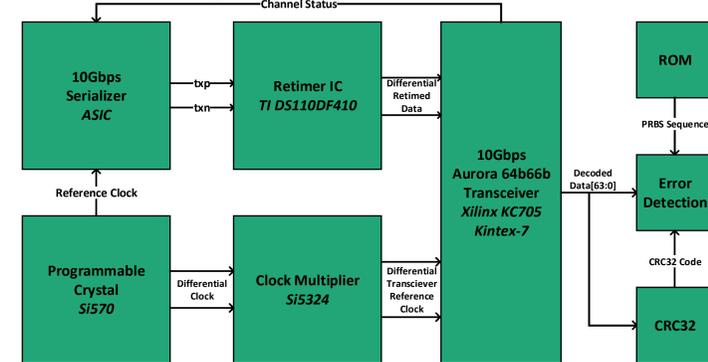
## Test System

- The sophisticated test system includes the following modules:
- TI DS110DF410 Retimer IC - Buffers bit-stream through resampling; this allows any previous channel effects to be reset.
  - SI570 Programmable Crystal IC – Generates a low jitter highly stable clock (Critical for high speed links); generated clock is used as a reference clock for the PLL in the ASIC.
  - SI5324 Clock Multiplier – Multiplies the previously generated reference clock to a frequency compatible for the reference clock of Xilinx's 10Gbps transceiver IP.
  - Xilinx KC705 FPGA (Aurora 64b66b 10Gbps Transceiver) – Receives the 10Gbps bit-stream, descrambles and decodes the data.
  - Xilinx KC705 FPGA (Synthesized Error Detection Code) – Checks the decoded bit-stream against defined bit-patterns generated on the ASIC. Debug software allows time-stamping when a bit-error is detected along with the difference in patterns.

## Retimer Debug Eye Diagram



## Test System Block Diagram



## CML Driver and Modelling/Simulation

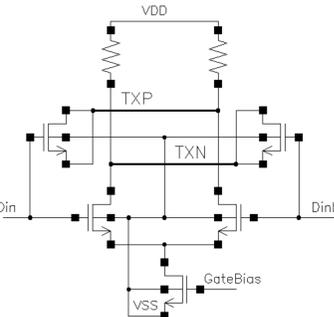
CML driver module:

- CML driver implemented using a standard CML architecture in 65nm and a 1.2V power supply.
- Counter charge injection transistors (half driver width) were added to correct the significant charge injected from the driver transistors due to a large gate to drain capacitance.

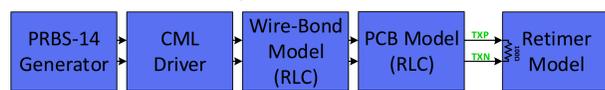
Simulated channel model includes:

- CML driver model: RLC extracted transistor model from Assura QRC tools
- Wire-bond model: RLC schematic model derived from first principles due to being fairly well understood geometry.
- PCB model: spice extracted model of the differential CML tracks on a preliminary test board PCB design with manufacturing properties included.
- Retimer Model: RC schematic with IC capacitor loads and the termination resistor.

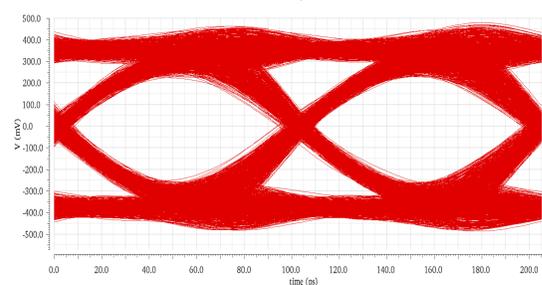
## CML Line Driver Schematic



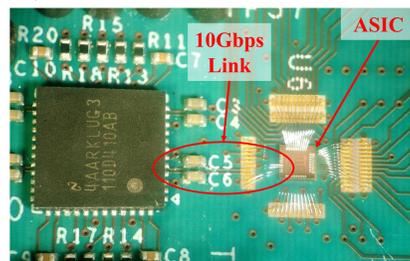
## Simulated Model Block Diagram



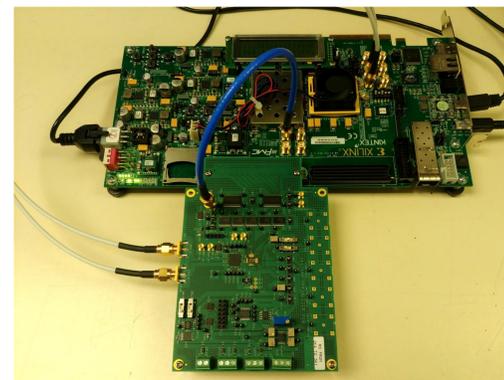
## Simulated Bit-stream 10.302Gbps



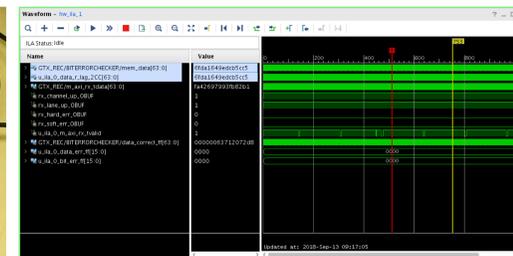
## Physical Channel



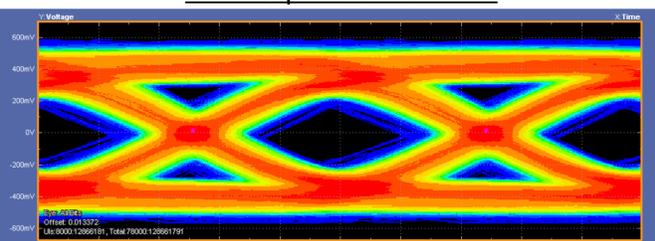
## Test System (Test Board + FPGA)



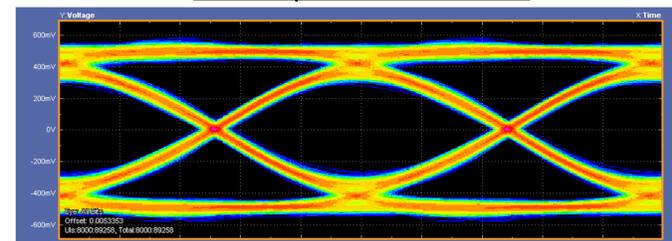
## Error Detection Software



## 10.302Gbps Bit-Stream ASIC



## 10.302Gbps Bit-Stream Retimer



## 5GHz Clock ASIC Output

