The Readout and Data Transmission of a Monolithic Active Pixel Sensor prototype for the CEPC Vertex Detector

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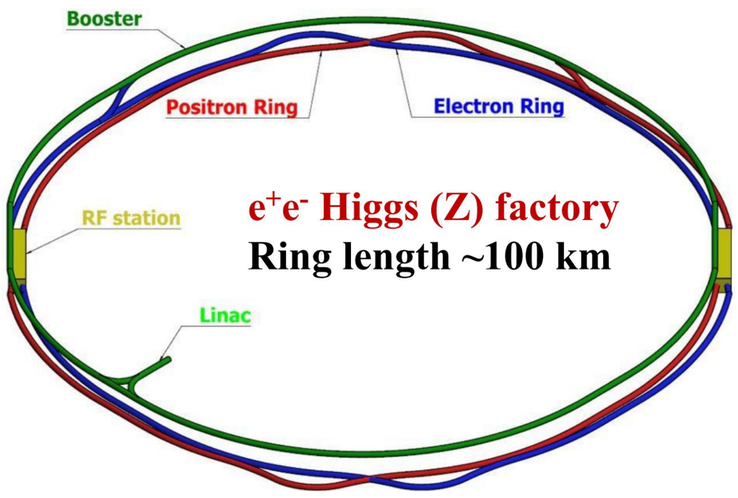
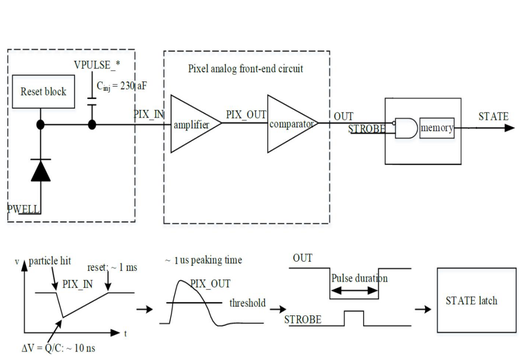
Introduction



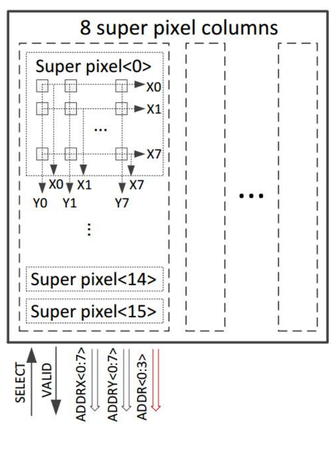
The Circular Electron Positron Collider (CEPC)

- The Circular Electron Positron Collider (CEPC) proposed by the Chinese high energy physics community in 2012 will be constructed in a tunnel with a circumference of ~100 km.
- The machine is expected to operate at the center-of-mass energy of ~240 GeV, with an instantaneous luminosity of 2 $\times 10^{34}$ $cm^{-2}s^{-1}$. CEPC will serve as a Higgs factory to measure the Higgs properties precisely.
- The machine could be later upgraded to a proton-proton collider with an unprecedented center-of-mass energy of ~100 TeV. CEPC will offer a unique opportunity for direct searches for New Physics in the high-energy range far beyond LHC reach.
- The vertex detector of CEPC requires low material budget, high spatial resolution, fast readout, and low power consumption.
- For the R&D of the CEPC vertex detector, we have developed a MAPS prototype MIC4 (MAPS In CCNU version 4) in TowerJazz 180-nm CMOS Image Sensor process.
- A new asynchronous data-driven readout architecture has been designed which combines the priority Address Encoder and Reset Decoder (AERD) scheme with the projection scheme.
- MIC4 contains a matrix of 128 rows by 64 columns with a pixel pitch of 25 μm.
- By a periphery priority encoder circuit and a data readout and framing circuit, MIC4 readouts data real time without on-chip memory.
- An 8B10B encoder, a 10:1 serializer, and an LVDS driver are implemented to transmit serially the data at 1.2 Gbps.

The design of AISC

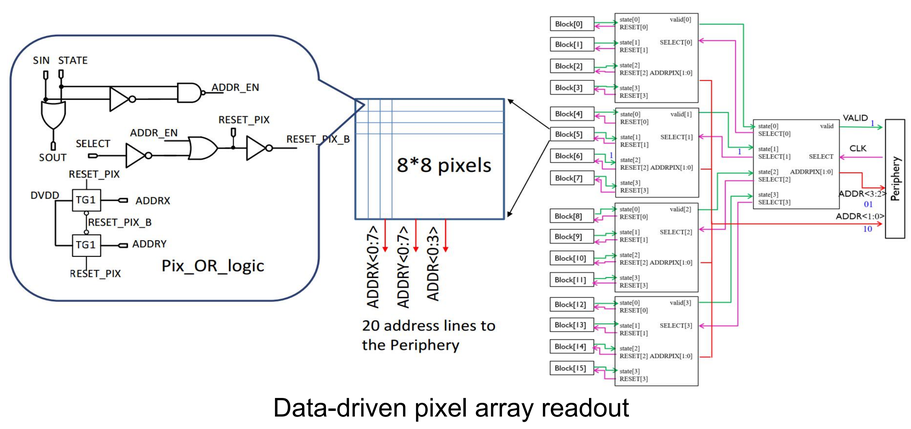


Pixel structure

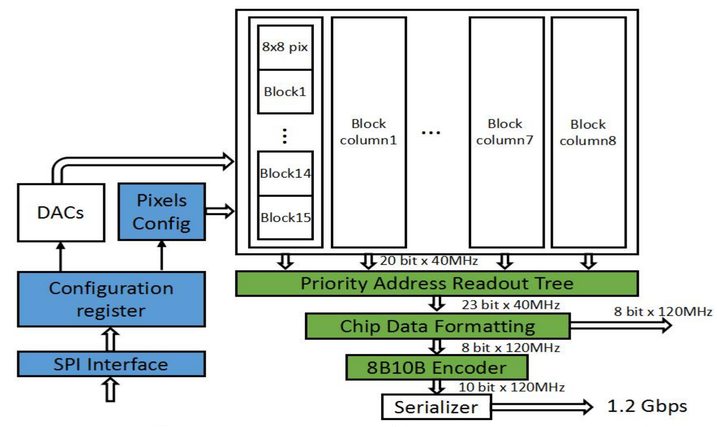


- MIC4 contains a matrix of 128 rows by 64 columns with a pixel pitch of 25 μm.
- The matrix is divided into Super Pixels of 8 × 8 pixels.
- Thus MIC4 has 8 Super Pixel columns, each column containing 16 Super Pixels.
- Each Super Pixel uses the two-dimension projection (X and Y directions) to identify the address of each hit pixel based on a OR-gate chain circuit.
- Each Super Pixel column uses an asynchronous AERD circuit to stream the data from the pixels to the periphery.

- Each pixel contains a sensing diode, an amplification, a discriminator, and a hit storage register connected to a sparsified readoout circuitry.
- Peaking time < 1 μs, pulse duration < 3 μs, with power consumption of 110 nW/pixel.
- ENC: ~8 e-.
- Pixel size: 25um × 25um.



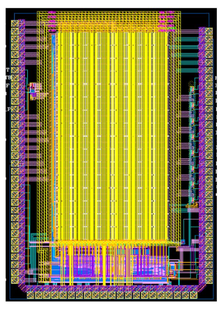
Data-driven pixel array readout



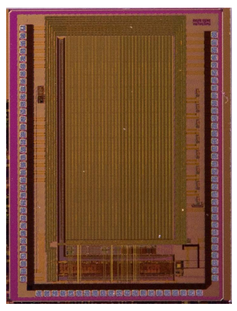
The block diagram of the periphery readout

- In the periphery of MIC4, a periphery-AERD (PAERD) circuit has been implemented to identify the addresses of 8 Super Pixel columns.
- PAERD receives 20 address bits from each Super Pixel column and adds additional 3 bits to form a 23-bit pixel address.
- A Data ReadOut and Framing circuit (DROF) interacts with PAERD to read the hit pixel address at the rate of 40 MHz/hit.
- DROF is also responsible for forming data frames. The frame has 384 bits, including an 8-bit comma word K28.5 as the frame header and an 8-bit frame trailer to identify the number of valid data in the payload.
- No large memory is used to store frames and only a small FIFO is used to convert the data bit width.
- MIC4 has two means of data transmission, a 120 MHz parallel data port that directly reads out the 8-bit data from the FIFO and a 1.2 Gbps serial transmission port that is implemented by an 8B10B encoder, a 10:1 serializer, and an LVDS driver in the periphery.

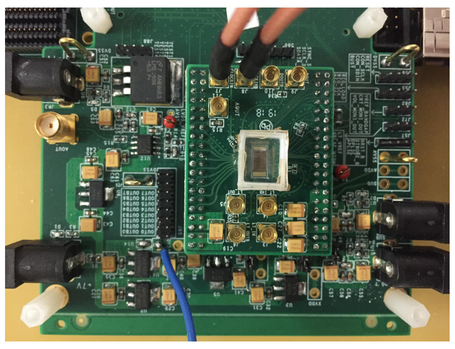
The test system and measurement results



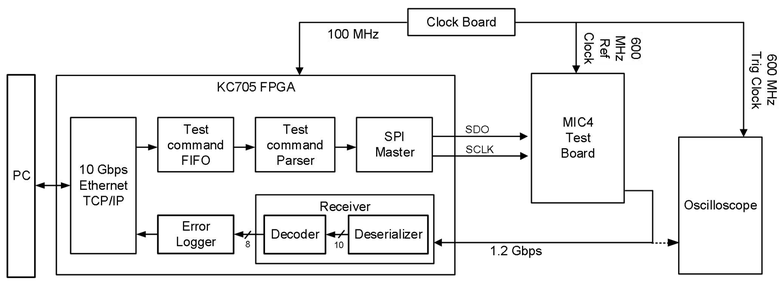
Layout of MIC4



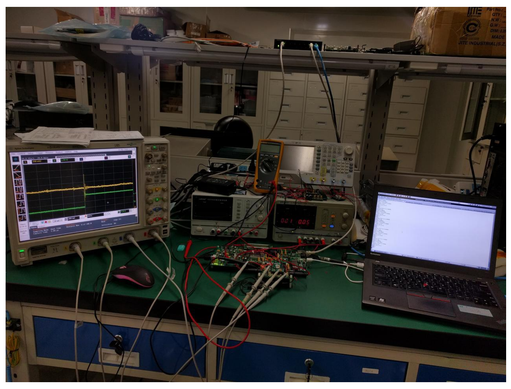
A picture of MIC4



A picture of bonding board and test board



The block diagram of test setup



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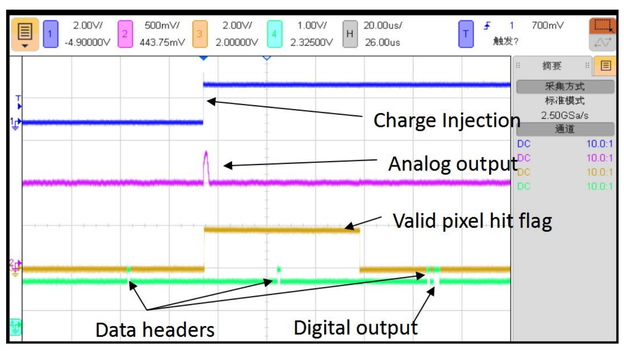
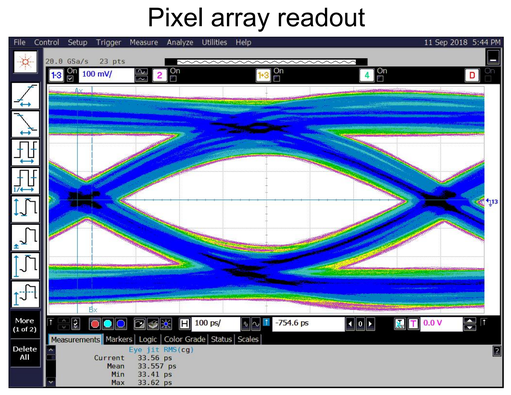


Pixel array readout



output eye diagram at 1.2Gbps

Conclusion

- For the R&D of the CEPC vertex detector, we have developed a MAPS prototype MIC4 in TowerJazz 180-nm CMOS Image Sensor process.
- New data-driven readout architecture is implemented to achieve high spatial resolution, fast readout, and low power consumption.
- By a periphery priority encoder circuit and a data readout and framing circuit, MIC4 readouts data real time without on-chip memory. An 8B10B encoder, a 10:1 serializer, and an LVDS driver are implemented to transmit serially the data at 1.2 Gbps.

Acknowledgments

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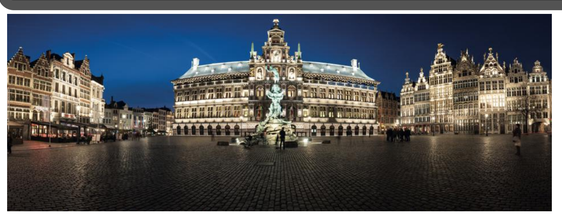

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