Contribution ID: **113** Type: **Poster**

The Readout and Data Transmission of a Monolithic Active Pixel Sensor prototype for the CEPC Vertex Detector

Tuesday, 18 September 2018 18:35 (15 minutes)

We present the readout and data transmission of a MAPS prototype MIC4 for the R&D of the CEPC vertex detector. New data-driven readout architecture is implemented to achieve high spatial resolution, fast readout, and low power consumption. MIC4 contains a matrix of 128 rows by 64 columns with a pixel pitch of 25 μm. By a periphery priority encoder circuit and a data readout and framing circuit, MIC4 readouts data real time without on-chip memory. An 8B10B encoder, a 10:1 serializer, and an LVDS driver are implemented to transmit serially the data at 1.2 Gbps.

Summary

The vertex detector of the Circular Electron-Positron Collider (CEPC) requires low material budget, high spatial resolution, fast readout, and low power consumption. The Monolithic Active Pixel Sensor (MAPS) as the most promising candidate technology has been chosen to satisfy all those requirements. For the R&D of the CEPC vertex detector, we have developed a MAPS prototype MIC4 in TowerJazz 180-nm CMOS Image Sensor process based on new asynchronous data-driven readout architecture that combines the priority Address Encoder and Reset Decoder (AERD) scheme with the projection scheme.

MIC4 contains a matrix of 128 rows by 64 columns with a pixel pitch of 25 μm. Each pixel contains a sensing diode, an amplification, a discriminator, and a hit storage register connected to a sparsified readout circuitry. The matrix is divided into Super Pixels of 8 × 8 pixels. Thus MIC4 has 8 Super Pixel columns, each column containing 16 Super Pixels. Each Super Pixel uses the two-dimension projection (X and Y directions) to identify the address of each hit pixel. Each Super Pixel column uses an asynchronous AERD circuit to stream the data from the pixels to the periphery.

In the periphery of MIC4, a periphery AERD circuit called PAERD has been implemented to identify the addresses of 8 Super Pixel columns. PAERD receives 20 address bits from each Super Pixel column and adds additional 3 bits to form a 23-bit pixel address. A data readout and framing circuit called DROF interacts with PAERD to read the hit pixel address at the rate of 40 MHz/hit. DROF is also responsible for forming data frames. The frame has 384 bits, including an 8-bit comma word K28.5 as the frame header and an 8-bit frame trailer to identify the number of valid data in the payload. No large memory is used to store frames and only a small FIFO is used to convert the data bit width. The DROF writes in real time the 23-bit-width hit pixel address to the FIFO at the rate of 40 MHz and inserts the frame header and the frame trailer according to the frame definition. MIC4 has two means of data transmission, a 120 MHz parallel data port that directly reads out the 8-bit data from the FIFO and a 1.2 Gbps serial transmission port that is implemented by an 8B10B encoder, a 10:1 serializer, and an LVDS driver in the periphery.

MIC4 is being evaluated. The test system consists of a test board, a Kintex-7 FPGA, and control software. The FPGA implements an SPI master to configure MIC4, a deserializer to convert the serial data into the parallel data, an 8B10B decoder to recover the original data, and a 10Gbps TCP/IP module to receive test commands from the control software on a PC and transmit original data to the PC. Preliminary tests show that the readout and parallel data transmission work properly. The serial data transmission test will be carried out in the coming months and will be presented in the workshop.

Primary authors: XIAO, Le (Central China Normal University); Mr YOU, Bihui; Prof. SUN, Xiangming; Prof. HUANG, Guangming (Central China Normal University); YANG, Ping

Presenter: XIAO, Le (Central China Normal University)

Session Classification: Posters

Track Classification: ASIC