A 65 nm Data Concentration ASIC for the CMS Outer Tracker Detector Upgrade at HL-LHC

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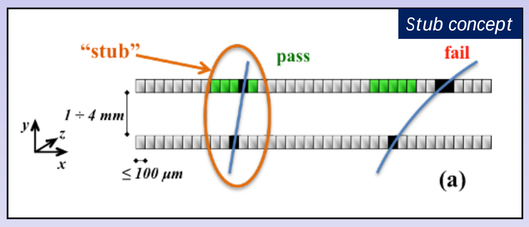
Introduction

Next generation of chips at **High-Luminosity LHC** (HL-LHC) will be exposed to extremely high levels of radiation and particle rates. In the so-called **Phase II upgrade**, the CMS experiment will need a completely new tracker detector: the main goal is to make sure that physics performance stay stable with respect to the current detector.

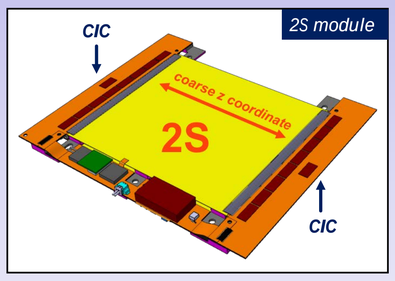
It will be included in the first level of the trigger chain, which runs at **40 MHz**. To ensure tracker data extraction at 40 MHz, a new type of detection module has been designed.



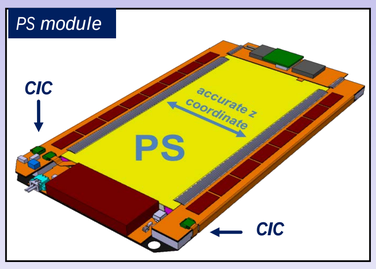
- Future tracker module (aka **p_T-module**) detection area is a superposition of 2 silicon sensors.
- A charged particle crossing a module creates two correlated clusters, which are reconstructed within the module to form **a stub.**
- Stub width is called the ***bend*.** Bend is linked to the particle transverse momentum (p_T). For track trigger, only low bend stubs are necessary.
- Reducing data rate by one order of magnitude, **stubs make tracker data extraction @40MHz possible.**

2 front-end flavours:

Tracker will be populated with **2 pT-module types: PS (pixels/strips) and 2S (strips/strips).**



- FE readout chains are differents (changes are in the FE-ASICs, hybrids, data formats). **CIC ASIC is the only shared component**.
- There will be 2 CIC chips per module.

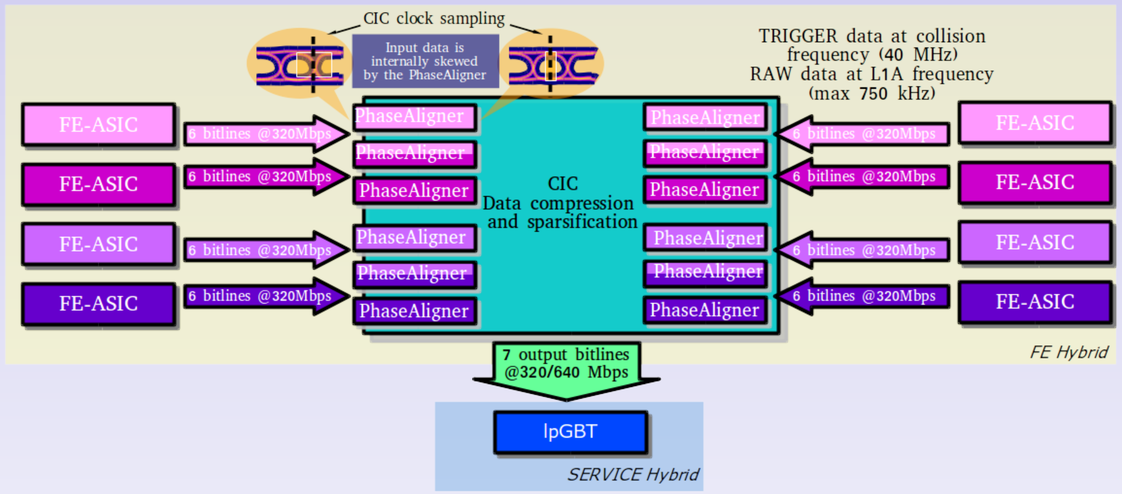


Concentrator integrated circuit (CIC)

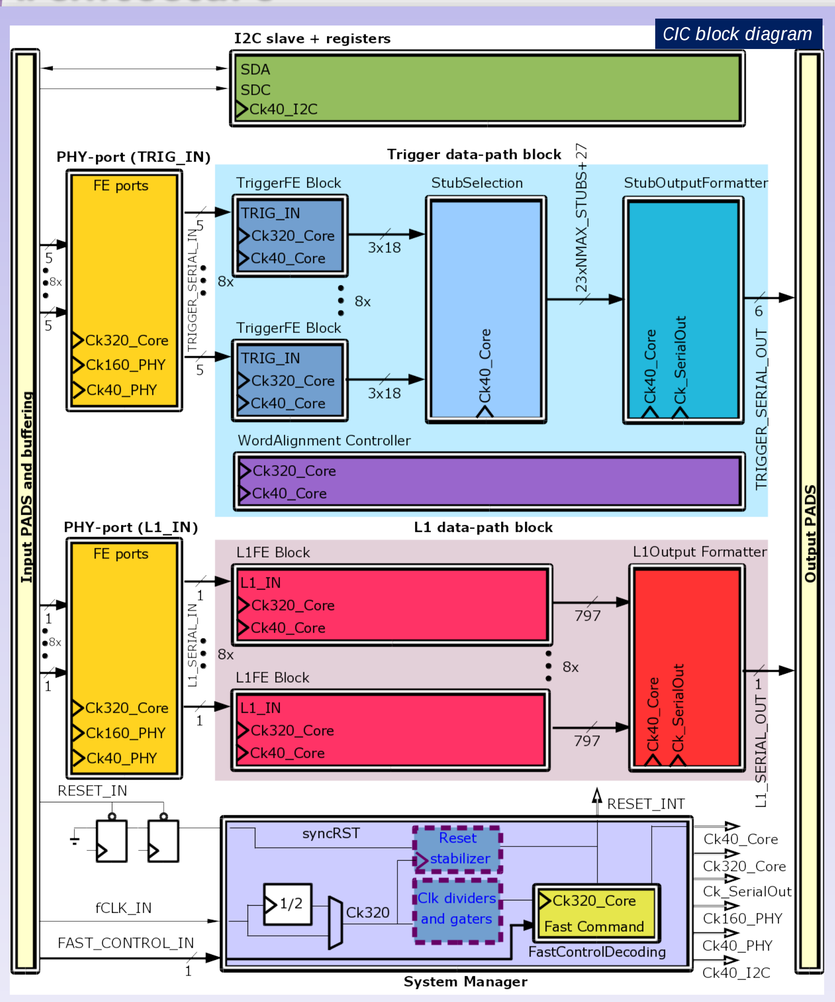
- A front-end chip **common to PS and 2S modules** of the future Phase-II CMS Outer Tracker.
- **It collects the digital data** coming from 8 upstream FE chips (MPAs[1] or CBCs), it **formats the signal in data packets** containing the trigger information from 8 bunch crossings and the raw data from events passing the first trigger level, and finally it **transmits** them to a lpGBT[2] chip.
- It receives inputs from 48 lines at 320 Mbps with **2 different data formats.**
- It sends outputs through 7 lines at 320/640 Mbps using **one single data format.**
- The design and implementation is in a **65nm CMOS technology**.
- Chip core works at **2 different input voltages**: either at **1.0 V** (PS) or **1.2 V** (2S).
- A first prototype of CIC will be submitted by the **end of September 2018**.
- The second run of CIC (including SEU hardened design) is foreseen by the **end of 2019**.

CIC role in the readout chain

- 2 data streams are generated in the Front-End hybrid for the Back-End:
  - **L1 data**: stream of frames responding to the L1-accept trigger signal. Each frame aggregates the hit cluster data received from all FE chips. Frame size is flexible and depends on the number of hits in the module. The sustainable capacity (per CIC chip and per L1-accept event) is **254 clusters** (@ PS) and **127 clusters** (@ 2S).
  - **TRIGGER data: se**quential stream of 8 BX long blocks. Each block contains the Trigger data aggregated from the 8 FE chips associated to one CIC. The CIC can select and forward up to **40 stubs** among the 192 potential input stubs.
- CIC provides to the readout chain an extra factor 10 of data reduction, by **grouping data over time (8 BX blocks)** and **space (8 input chips)**.
- CIC ASIC uniforms the **data format** for the Back-End.



Architecture



- ***Phase Aligner*:** analog IP block used at each input data channel incoming from the 6 lines from each MPA/CBC front-end. Is required in order to synchronize the signal with the internal clock (320 MHz).
- ***CIC_Core*:** based on two independent data paths, working in parallel:
  - ***Trigger data path*:** treatment of data payload produced @ 40MHz (*deserialization, word alignment, stub selection and output frame creation*). This is the information necessary to the L1 track trigger.
  - ***L1 data path*:** treatment of raw tracker data produced @ 750kHz max. (*sparsification in the case of CBC, storage in FIFOs, output frame creation*). This data payload is sent on request each time an L1-accept signal is received.
- ***SystemManager*:** manages the clocks generation (***40 MHz, 320 MHz, 640 MHz***), clock gating, reset distribution, command decoding from the fast control frame.
- ***SlowControl*:** manages the communication via I^2C protocol for control and monitoring of the system. It contains the I^2C slave and the internal slow control registers.

IPs blocks: Phase aligner (***SMU Univ. and CERN***), SLVS Drivers and receivers[3] (***INFN and Univ. Bergamo and Pavia***), CMOS I/O pads and I^2C Slave (***CERN***), ESD protections (***SOFICS***).

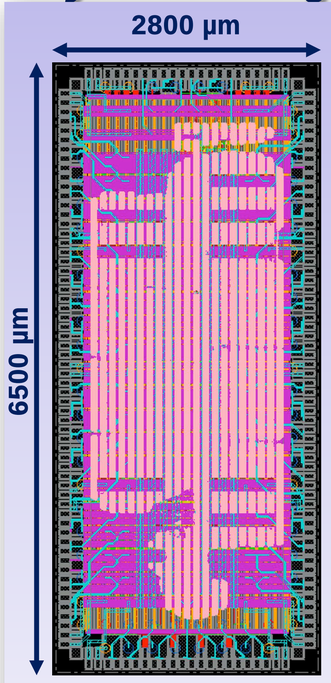
TRIGGER DATA PATH:

- Trigger readout data is **synchronous** across all the detector with respect to the LHC BX clock.
- CIC output trigger frame contains data from:
  - *64 input CBC frames or 32 input MPA frames.*
- Differents configurable output formats:
  - *320 Mbps or 640 Mbps via 5 or 6 (configurable) output lines;*
  - *Z information (MPA), bend on 3 bits (MPA), 4 bits (CBC) or no bend forwarding;*
- If the output frame is too short to send all the stubs, **lowest |bend| stubs are transmitted in priority.**
- Stubs sorting network is based on comparators/switchers optimized to reduce the sequential comparisons.

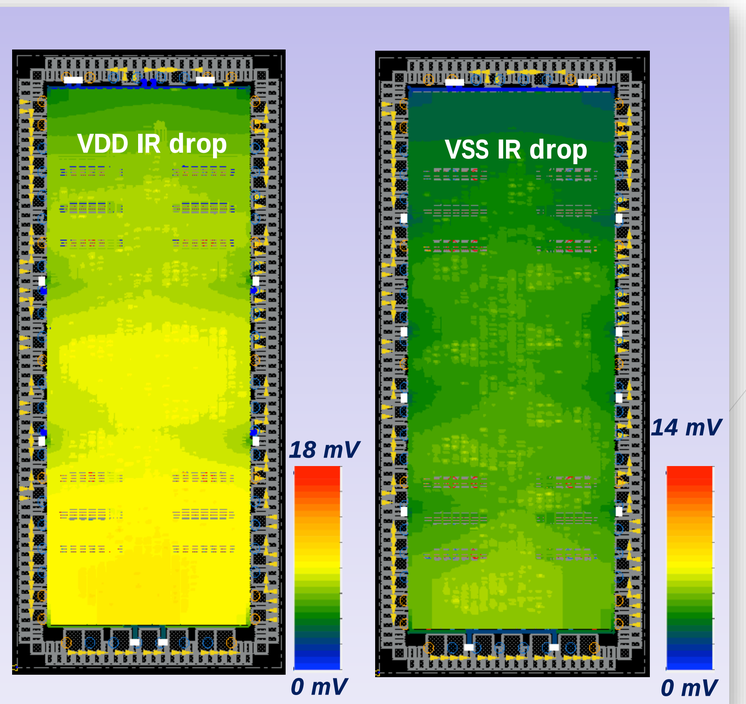
L1 DATA PATH:

- L1 readout data is **asynchronous** between different modules and CIC internal processing starts after reception of the L1-accept signal.
- Each FE block handles frame reception independently from the others.
- L1 output formatter merges the data that corresponds to the same event.
- The readout data from CBC (2S module) is sparsified in the CIC ASIC.

Physical design

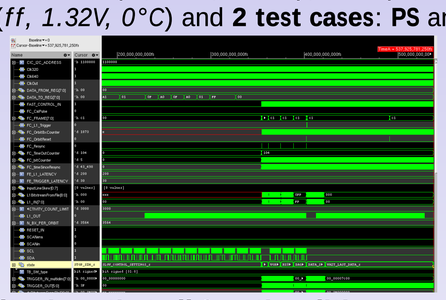


- Process **TSMC 65nm LP 1p7m4x1z1u** metal stack.
- **Wire bond** with AP RDL.
- **~372k** standard cells.
- Periphery ring:
  - **48 sLVS RX pads** along the left and right sides (core+periphery supplies)
  - **7 sLVS TX pads** (*on the bottom side*) & **2 sLVS RX + 7 CMOS** pads (*on top side*)
- **Bare die,** bumped ASIC (*flip chip*) with C4 bumps.
- Top level **power routing**:
  - 8 vertical stripes in AP layer
  - 312 horizontal stripes in M7 (ultra thick) layer
- **Periphery supply**:
  - The power routing of the periphery supply is being kept separate from the core
  - Radiation tolerant ESD protections used in periphery ring
- **Power estimation (***worst corner*):
  - PS @ 1.1V: **312 mW** (*setup mode*); **288 mW** (*running mode*)
  - 2S @ 1.32 V: **443 mW** (*setup mode*); **415 mW** (*running mode*)



Standalone Testbench

- **Test design functionalities** within a script-based framework (*python*).
- It performs the **comparison** between data stream from CMS simulation environment with the CIC model output after the phase alignment and data treatment.
- Back-annotated simulations are performed in **3 corners**: **MAX** (*ss, 0.9V, -40°C*), **TYP** (*tt, 1V, 25°C*), **MIN** (*ff, 1.32V, 0°C*) and **2 test cases**: **PS** and **2S**.



- **Results show that all functionalities are met .**
- System level Testbench for the validation of the full acquisition chain, developed at CERN (***S.Scarfi's poster***).

We want to thank D.Ceresa, A.Caratelli, K.Kloukinas for their contribution in this project.

[1] A 65 nm pixel readout ASIC with quick transverse momentum discrimination capabilities for the CMS Tracker at HL-LHC, D.Ceresa et Al., JINST, Vol 11, Jan '16.
[2] https://espace.cern.ch/GBTProject/LpGBT/Specifications/LpGbtxSpecifications.pdf
[3] Design of low-power, low-voltage, differential I/O links for High Energy Physics applications, *G. Traversi et Al,* JINST Vol. 10, Jan. '15.

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