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A 65 nm Data Concentration ASIC for the CMS Outer Tracker Detector Upgrade at HL-LHC

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The concentrator integrated circuit (CIC) is a front-end chip for both PS and 2S modules of the future Phase-II CMS Outer Tracker upgrade at the High Luminosity LHC (HL-LHC). It collects the digital data coming from eight upstream FE chips (either MPAs or CBCs) format and transmit it to the LpGBT unit. The design and implementation in a 65nm CMOS technology of the first prototype are presented.

Summary

The concentrator integrated circuit (CIC) is a front-end chip for both PS and 2S modules of the future Phase-II CMS Outer Tracker upgrade at the High Luminosity LHC (HL-LHC). It collects the digital data coming from eight upstream FE chips (either MPAs or CBCs, depending on the module type), formats the signal in data packets containing the trigger information from 8 bunch crossings and the raw data from events passing the first trigger level, and finally transmits them to the LpGBT unit. The design and implementation in a 65nm CMOS technology of the first prototype ASIC that integrates all data transmission functionalities for system level operation are presented in this contribution.

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