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The Quality-Assurance Test of the ATLAS New Small Wheel Read-Out Controller ASIC

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The Read-Out Controller (ROC) ASIC will be used to store, de-randomize, aggregate, filter and form complex packets with the digitized data coming from the New Small Wheel (NSW) muon detectors of the ATLAS experiment. The ASIC test setup is based on a Xilinx Kintex Ultrascale FPGA evaluation board, implementing input data streams emulators and output data analyzers for functional verification which are controlled and monitored by a MicroBlaze microprocessor. Jitter and skew of the ASIC's PLL outputs are measured using the FPGA transceiver eye-margining circuits. The design validation, test procedure and quality-assurance mass-testing results are presented.

Summary

The Read-Out Controller (ROC) is a custom packet processor ASIC implemented in 130 nm CMOS technology. The ROC will be used to store, de-randomize, aggregate, filter based upon an additional level of trigger and form complex packets with the digitized data coming from the New Small Wheel (NSW) muon detectors within the ATLAS experiment. In addition, the ROC distributes clocks and TTC (Time Trigger and Control) signals to companion front-end chips providing fine skew and latency control. The circuit is designed to work in both Phase-I and Phase-II environments being compatible with either one or two-level trigger scenarios.

For testing the first ROC dies and validate the design a test environment was developed using a Xilinx Kintex Ultrascale KCU105 FPGA evaluation board and a custom test board with FMC (VITA-57) interface. First version of this board provides external access to the phase adjustable clocks generated by the ROC PLLs and the decoded TTC signals in order to be measured with an oscilloscope or logic analyzer. This allows measurement of clock jitter and propagation delays with metrological accuracy. All other signals connected to the ROC packet processor core are routed to the test FPGA. Early versions of this board with the ROC wire-bonded directly on the PCB, or with an intermediate QFP package with partial pad coverage were used for early design validation.

The second version of the test board uses a second FMC connector and connects the clocks and TTC signals generated by the ROC to FPGA high-speed transceivers and fabric pins, respectively. This allows for complete automatic test coverage of the ASIC, including jitter and skew evaluations, without the use of external measurement devices. The board includes programmable regulators, current and voltage monitors for power margining tests and power consumption characterization. It uses an open-top easy-insertion BGA socket in order to be used for mass-testing of the 8-10,000 ROC ASICs needed for the experiment.

The FPGA firmware contains packet generators emulating the ROC input data streams, a TTC stream emulator and two I2C masters for chip configuration and control. The frequency of the input data packets can be configured from 100 kHz up to 1400 kHz in 100 kHz steps. For each frequency the percentage of empty packets and the average size of the non-empty packets can be selected from predefined values. The content and size of the packets are deterministic, different for each generator. Specific patterns can be programmed that allow the filling and verification of the ROC memory buffers. Firmware-based output data analyzers check all the ROC output data for encoding, coherency, parity, checksum and content errors. All these modules are controlled and monitored using a MicroBlaze soft-core. The embedded processor is also used to evaluate the jitter and skew of the programmable clocks with few-picosecond accuracy provided by FPGA de-serializers and in-system eye-scanning circuits.

This test environment was used for validation of the ROC implementation and is being used for mass-testing in the following period. The quality-assurance test procedure and test results will be presented.

Primary authors: MUON COLLABORATION, ATLAS (ATLAS); POPA, Stefan (Transilvania University of Brasov (RO)); MARTOIU, Sorin (IFIN-HH (RO)); LUCHIAN, Mihai (Transilvania University of Brasov - Romania); COLIBAN, Radu Mihai (Transilvania University of Brasov (RO)); IVANOVICI, Mihail (Transilvania University of Brasov (RO))

Presenter: POPA, Stefan (Transilvania University of Brasov (RO))

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