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ASoC: A High Performance Waveform Sampling and Feature Extraction System-on-Chip for Data Acquisition

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Readout electronics for modern particle imaging based identification detectors must be compact, low power, deliver acceptable timing resolution and be robust to pile-ups. The solution is to integrate full waveform sampling, analog buffering and feature extraction and digital signal processing into one single Application Specific Integrated Circuit (ASoC in the following). ASoC can be used as a building block for such readout devices. The prototype fabricated ASoC has 4 channels, operates at 3 GSa/s and has on-chip trigger timestamping, calibration and signal processing capabilities. ASoC also provides 8k storage samples per channel which makes it suitable for large experiments.

Summary

Modern imaging based particle identification detectors require design and implementation of data acquisition systems capable of tracking and recording data from fast moving particles. In large large collider experiments, collisions happen at tens to hundreds of thousand events per second. This translates to a need for sub-detectors with tens of thousands of channels operating under power constrained and compact conditions. An example of such sub-detectors is the Belle II DIRC based Time of Propagation (TOP) Particle Identification Detector also known as iTOP. The core of the readout electronics for such detector consists of full waveform sampling IRSX ASICs developed at the University of Hawaii delivering 35ps timing resolution. The IRSX ASIC and the accompanying Zynq based FPGAs are assembled on board stacks and directly attached to MCP-PMTs. Processing and feature extraction within the front-end allows robustness to pile-up events while reducing the number of cables for back-end connections. Given that the entire assembly is located inside the superconducting magnet, thermal dissipation becomes an issue. Based on this experience in instrumenting the readout electronics for the TOP detector and while the equipment performed beyond expected performance, there is an opportunity to integrate more custom electronics into a single chip to further reduce power and cost and enhance the performance.

The Analog to digital converter System-on-Chip (ASoC) is the first step toward higher integration. In this project we developed the ASoC by integrating into one SoC (i) analog signal conditioning circuits, (ii) an optimized version of IRSX, and (iii) digital readout and signal processing block capabilities (triggering, sparsification and data reduction). As it is demonstrated in this summary, adding the digital capabilities to the ASoC reduces the need for costly high performance Field Programmable Gate Arrays (FPGAs) which reduces backend data congestion, power dissipation and deployment complexity. We have demonstrated that ASoC as such reduces the cost per channel to a quarter of the current available solutions for large detectors making it especially attractive for large experiments.

We designed ASoC to operate at 3GSa/s in a low cost 250nm CMOS process. The chip also has a deep buffer of 8k samples which is valuable for large experiments with large trigger delay. The prototype ASoC is fabricated and testing and evaluation has been performed on both the analog and digital sides of the chip. Region of Interest readout on various types of delayed pulses has been performed and operation at 30kHz and above trigger rate readout has been confirmed. On-chip calibration and processing is done through synthesized logic which allows for a user-friendly interface with the backend.

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