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Design of HVCMOS pixel sensor ASIC with on-chip readout electronics for ATLAS ITk Upgrade

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High Voltage CMOS (HVCMOS) pixel sensor ASICs are engineered to meet the requirements of ATLAS ITk pixel barrel outer layers for LHC high luminosity upgrade. This work presents the design of HVCMOS sensor ASICs with emphasis on the readout system architecture and Digital Control Unit (DCU) design. The on-chip readout system introduces an efficient data transfer scheme from pixels to chip periphery. The data links work at a rate of 1.6Gbps which has been achieved by a novel serializer scheme. The test beam results on a large area AMS 0.18µm prototype without triggered readout shows more than 99% readout efficiency.

Summary

High Voltage CMOS (HVCMOS) pixel sensor ASICs are the building blocks of the planned HVCMOS quad module which is a low cost alternative to existing hybrid modules for ATLAS Inner Tracker (ITk) pixel barrel outer layers. . The main blocks of HVCMOS ASICs are sensor array, trigger buffers, Digital Control Unit (DCU) and PLL. The HVCMOS sensors use deep n-wells as charge collecting pixel electrodes. The pixel electronics (charge sensitive amplifier and a discriminator) is placed inside the n-wells. High voltage is used to deplete the substrate underneath. The use of large charge collecting electrodes (large fill-factor) and a high resistive wafer ensure high signal amplitudes. The sensors are radiation tolerant up to 100 MRad. The signals caused by particle hits are digitized and transferred to the digital periphery of the ASIC. The pixel signals are transmitted to trigger buffers which contain SRAM memory arrays and readout logic. The buffer acts as a storage for particle hit information until the trigger latency elapses. The readout logic is responsible for filtering the triggered hits and marking them for readout. The marked hits are sorted in a chronological order of events. The digital control unit (DCU) forms the brain of HVCMOS ASIC which schedules the data transfer from trigger buffer until the data are serially transmitted off chip. The data links work at a rate of 1.6Gbps which has been achieved by a novel serializer scheme. This contribution presents the design of HVCMOS sensor ASICs with major focus towards the readout architecture and data transmission. Test beam measurements conducted at different facilities on 0.18 µm HVCMOS large area (0.3 cm x 1.9 cm) prototypes without trigger buffers show a readout efficiency of more than 99%. An overview of the laboratory tests and test beam results will be presented.

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