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The Quality Assurance of two ASICs for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade

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We present the quality assurance (QA) test of a dual-channel Vertical-Cavity Surface-Emitting Laser (VCSEL) driver ASIC LOCld and a low-latency, low-overhead dual-channel transmitter ASIC LOCx2 for the ATLAS Liquid Argon Calorimeter Phase-I upgrade. In the QA test, we screen about 7200 LOCld chips and 7200 LOCx2 chips to ensure their basic functionality. All tests are automatically conducted and controlled by LabVIEW software running on computers. The QA test systems and test results for the two ASICs are reported.

Summary

The ATLAS Liquid Argon Calorimeter (LAr) Phase-I trigger upgrade requires high-speed, low-latency data transmission to read out the data from the LAr Trigger Digitizer Board (LTDB). To meet this requirement, two ASICs, LOCld and LOCx2, have been designed. LOCld is a dual-channel Vertical-Cavity Surface-Emitting Laser (VCSEL) driver ASIC, each channel operating at up to 8 Gbps. LOCx2 is a dual-channel transmitter ASIC, each channel operating at 5.12 Gbps. LOCx2 can accommodate data from three types of ADCs, an ASIC ADC and two Commercial-Off-The-Shelf (COTS) ADCs. About 7200 LOCld chips and 7200 LOCx2 chips have been produced. In order to ensure their basic function before assembly, a Quality Assurance (QA) test must be conducted.

In the QA test of LOCld, we check eye diagrams, register configuration, power consumption, and bias currents. We test two chips simultaneously for about 5 minutes. We have tested all about 7200 chips. The failure rates are 6.44% for power consumption failure, 9.31% for register configuration failure, 5.1% for eye mask failure, 7.24% for bias current failure, respectively. The test results show that the overall yield is about 71.86%, satisfying the need of the ATLAS LAr Phase-I upgrade.

In the QA test of LOCx2, we measure eye diagrams and the Bit Error Rate (BER) of each chip. We also plan to sample about 5% of the chips that pass the above tests in each wafer to measure the Phase-Locked-loop (PLL) tuning range, the jitter of the serial output, and the 3.125-ns input signal skew tolerance in the ASIC ADC mode. The QA test system has two setups. The first setup is for eye diagram and the PLL tuning range tests. The eye diagram and the serial output jitter are observed on the 5.12-Gbps serial output signals. The PLL tuning range is measured on the PLL output signal with the adjustable input clock frequency. The second setup is for the BER and input signal skew. We measure the BER test under the combination of three different power supply voltages (2.25 V, 2.5 V, 2.75 V) and three ADC types. The BER test is the most time-consuming part. In order to shorten the BER test time, a QA test system has been developed so that six chips are tested simultaneously. The system includes a commercial FPGA evaluation board Xilinx KC705, two printed circuit boards (PCBs), firmware implemented in the FPGA, and software written in LabVIEW. KC705 is used in the system as ADC data generators and the data link receivers with error loggers. We have tested about 200 chips for BER and about 300 chips for eye diagrams so far. All the 7200 LOCx2 chips will be tested in this summer. The test result will be presented in the workshop and the proceeding.

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