Contribution ID: **34** Type: **Poster**

A rad-hard full information pixel imager chip for the HEPS-TF project

Tuesday, 18 September 2018 18:35 (15 minutes)

A pixel chip based on the Hit-Driven scheme was designed for the HEPS project in China. The full information of every photon, including the hit position, arrival time, and photon energy, are detected by the ToT method. Thus a 3D animation of clusters can be rebuild. Priority arbitrary logic was designed to readout all the hit pixels sequentially to the column FIFO, and the chip overall buffer. The beamline gate signal was used for trigger to make the level 1 data selection. A full functional chip was taped out and proved. It also survived after 100 Mrad X-ray irradiation.

Summary

The High Energy Photon Source (HEPS) is the next generation of synchrotron radiation light source in China, and the Test Facilities (TF) initiates all the R&Ds. A new concept was proposed from the beamline requirement for X-ray pixel imaging detectors that full information of every photon, including its hit position, arrival time, and photon energy, are to be recorded. Then one can use these information to rebuild a 3D animation of every cluster's dynamics. This provides possibilities for experiments with sparse events, while have special interests on dynamic processes.

A hybrid pixel detector with a 300-um-thick silicon P-in-N sensor are designed. To keep the pixel compact with small size, the ToT (Time over Threshold) structure was used. The injection charge is converted to a triangular wave by a constant current source feedback of the charge amplifier. The width of the wave is proportional to the input charge. Then a discriminator and a TDC with global time stamps can easily digitize the analog output. Its leading edge gives the arrival time, and the time difference between the trailing and leading edge is proportional to the energy. Combined with an address encoder for pixel position, the full information of the event is thus acquired.

The pixel readout chip was designed in a Hit-Driven readout architecture for high hit rate. The pixel digital part was based on a FE-I3 like priority arbitrary logic. The time stamps of both edges will be latched in pixel registers, and the hit flag will be sent by the Fast-Or bus to the periphery. Once a pixel was hit, the full column will be froze for new hits. With a readout acknowledgement from the End-of-Column (EoC) logic, the latched bits of hit pixels, including two 8-bit time stamps of both edges, plus 8-bit address, will be sequentially readout to the EoC buffer, validating by priority token. After the hit flag was clear, this column was released for the new hits.

The EoC event buffer was designed in a Looped-FIFO style. Its depth was designed to be 64 words to cope with most of the applications. All the non-empty EoC FIFOs, plus the column address code, will be further sent to the chip periphery FIFO in a similar priority logic. To make the data rate compatible with the output interface, trigger algorithm has to be implemented. The gate signal from the beamline is the best candidate. The chip receives the gate signal and records its time stamp. With the estimated trigger latency and gate width, the stored events whose arrival time stamps falls in the right time stamps region will be readout off chip by a high speed serializer; others are to be discarded.

A prototype pixel chip was designed and taped out by MPW using a CMOS 130nm technology. It integrates an 18*60 pixel array with full functionalities. The full chip was proved by thorough test. The X-ray irradiation result also showed the chip survived over a 100-Mrad dose, which is reliable enough for the synchrotron

radiation.

Primary authors: Dr WEI, Wei (IHEP, CAS); Dr FAN, Lei (IHEP, CAS); Dr REN, Jiayi (IHEP, CAS); Dr ZHANG, Jie (IHEP, CAS); Prof. WANG, Zheng (IHEP, CAS); Prof. JIANG, Xiaoshan (IHEP, CAS); Prof. ZHU, Kejun (IHEP, CAS); Prof. LIU, Peng (IHEP, CAS)

Presenter: Dr WEI, Wei (IHEP, CAS)

Session Classification: Posters

Track Classification: ASIC