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ABACUS : Two fast amplifiers for the readout of LGAD detectors

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The design of a single particle counter for therapeutical proton beams based on Low Gain Avalanche Diodes (LGADs) optimized for very fast signals is carried on in the framework of the INFN MoveIt research project. Fast signal shaping front-end electronics is mandatory in this application in order to deal with particle rates of the order of hundreds of MHz. Two preamplifier architectures, one based on a fast Charge Sensitive Amplifier with self-reset capabilities and a second one based on a Trans-Impedance Amplifier have been developed in a commercial CMOS 0.11 μm technology and submitted to the foundry.

Summary

The INFN MoVe-IT (Modeling and Verification for Ion beam Treatment planning) research project aims at developing models for biologically optimized treatment planning systems in proton beam therapy and dedicated devices for plan
verification.
In this framework a single particle counting detector and readout electronics for therapeutical proton beams is under development. The device will have to cope with fluxes up to 10ˆ9 cm2/s, while keeping the pileup probability below
1%. The detector is based on Low Gain Avalanche Diodes (LGADs) implemented with thin sensors (50 um) and gains of 10-20, thus optimized for very fast signals. The current prototype covers a 30x30 mmˆ2 area; currently two different sets of strip geometries are under evaluation.
The front-end electronics has to deliver not only fast rising times, as in timing measurement applications, but also a short signal duration in order to minimize the pile-up counting inefficiencies (instantaneous rates of 100 MHz or higher are expected in each readout channel). Moreover, in the energy range of therapeutical beams, the input charge dynamic range can be fairly large (between 3 and 150 fC) considering the large energy loss fluctuations in thin sensors.
Two different readout architectures have been developed in order to fulfill these demanding requirements. Both architectures, named ABACUS_v1a and ABACUS_v1b, have been designed in a CMOS 0.11 um technology and submitted to foundry on January 2018 in two different 24 channels test chips.
The first architecture is a high bandwidth TransImpedance Amplifier (TIA) based on a differential amplifier with resistive load and gain boost current sources, and a resistive feedback. Such schemes are commonly used for the readout of silicon photodiodes (PD) in optical receivers; however the typical PD capacitance is an order of magnitude lower than the one of the MoveIt LGADs and therefore it is more difficult to provide the required bandwidth with a sufficient transimpedance gain. Two flavours of this solution
have been designed and prototyped to address this issue : a two stage TIA and a single stage TIA driven by a current buffer. The first solution reduces the effects of the input capacitance by increasing the open-loop gain, at the expense of increase in power consumption and a slight decrease in
speed. The second solution decouples the detector from the gain stage, thus providing a lower sensitivity to the input capacitance. On the other hand, the buffer stage provides an extra contribution to the noise.
The second architecture is a fast Charge Sensitive Amplifier (CSA) based on a cascoded single ended amplifier with gain boost, followed by a comparator. In order to shorten the RC tail, a digital reset of the integrating

capacitor has been implemented. The reset signal is automatically generated by the output comparator; a recovery system has been implemented to keep the reset signal width sufficiently large to effectively discharge the capacitor. Local channel DACs have been implemented to fine tuning of the comparator threshold.
The discriminator output for both architectures drives a differential CML driver to maintain high signal rate.

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