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Design of a monolithic HR-CMOS sensor chip for the CLIC silicon tracker

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The CLIC Tracker Detector (CLICTD) is a monolithic pixel sensor chip targeted at the tracking detector of the Compact Linear Collider (CLIC). The chip features a matrix of 16×128 cells, each cell measuring $300 \times 30 \mu m^2$. The cells are segmented in the long direction in order to maintain the benefits of the small collection electrode. In the digital logic, a simultaneous 8-bit Time of Arrival and 5-bit Time over Threshold measurement is performed. The TowerJazz 180nm HR-CMOS Imaging Process was selected to fulfil the requirements of the CLIC silicon tracker. In this document the CLICTD design and chip interface are presented.

Summary

The CLIC Tracker Detector (CLICTD) is a monolithic pixel sensor chip designed according to the requirements for the silicon tracker of the Compact Linear Collider (CLIC) [1]. These requirements include a time measurement (Time of Arrival) with 8 bits range and 10ns time-tagging and an energy measurement (Time over Threshold) with 5 bits precision. A single point resolution of 7um in the transverse plane is required. The total material budget including supports, cables and cooling is 1-1.5% X0 per detection layer, allowing for ˜200um for silicon detector and readout. The average power consumption should be limited to 150mW/cmˆ2.

The TowerJazz 180nm CMOS imaging process has been chosen for this design, as it offers a deep P-well which allows to isolate the in-pixel digital logic from the collection electrode. The signal collection is done with a tiny collection electrode with very small capacitance. This minimises the noise in the front-end. A modification of this process includes an additional N-type implant that allows to fully deplete the epitaxial layer [2].

The unit cell of the CLICTD detector consists of an elongated pixel of 300×30umˆ2. In the analog part, the cell is segmented in eight front-ends, each one comprising a collecting diode, a charge sensitive amplifier, a discriminator and a 3-bit DAC used for local threshold tuning. Segmentation is required for prompt charge collection. The digital logic will store binary hit information for each of the front-ends. All eight discriminated outputs are combined by means of an "OR" gate. The combined output is then processed by the in-pixel digital logic, where a simultaneous 8-bit ToA and 5-bit ToT measurement is performed.

Due to the low duty cycle of the CLIC beam [3], the CLICTD matrix can benefit from a power pulsing scheme where the main power consuming nodes of the analog front-end are switched off between subsequent bunch trains. The average analog power consumption can therefore be minimised. Clock gating is implemented in order to minimise the power consumption in the digital logic.

The data is shifted out of the chip using a serial readout at a clock frequency of 40MHz. In order to reduce the amount of data that is shifted out of the chip, taking into account the expected maximum cell occupancy of ˜3%, a compression algorithm is implemented. A total of 22 bits is stored in each detector cell. If the compression algorithm is enabled, the data is shifted out only for the cells that have detected a hit. For cells that were not hit, only one bit will be shifted out.

The CLICTD prototype chip is currently in the final design stage. Although this design is done in the framework of the CLIC silicon tracker, it is expected to provide valuable input to different detector applications that could benefit from the selected process.

References:

[1] D. Dannheim, A. Nurnberg, CLICdp-Note-2017-002, 2017

[2] W. Snoeys et al., Nucl. Instrum. Meth. A 871 (2017) 90-96, 2017

[3] Physics and Detectors at CLIC: CLIC Conceptual Design Report, CERN-2012-003, 2012

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