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A Sigma-Delta ADC for Pixel Charge Readout Targeting Neutrinoless Double-Beta Decay Search in High-Pressure TPC

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We present a high resolution sigma-delta ($\Sigma\Delta$) Analog-to-Digital Converter (ADC) manufactured in a 0.35 μm CMOS process. The ADC consists of a cascaded $\Sigma\Delta$ modulator and a SINC4 decimation filter. Tests show that the ADC achieved a 80 dB signal-to-noise ratio and a 14 effective number of bits with a 25.6 MHz sampling clock at a 200 kHz input signal. Its characteristics are uniquely suited for high-pressure TPC readout that focuses on high energy resolution.

Summary

The discovery of neutrino oscillation confirms that neutrinos have small but non-zero masses. However, the absolute mass of neutrino is yet to be determined. And a more fundamental question, whether neutrinos are their own anti-particles, i.e. Dirac or Majorana, is yet to be answered as well. The observation of Neutrinoless Double-Beta Decay ($0\nu\beta\beta$) would unambiguously prove that neutrinos are their own anti-particles (Majorana) and provide a measure of the absolute neutrino mass. The experimental signature of $0\nu\beta\beta$ is two energetic electrons with the energy sum that equals the $Q_{\beta\beta}$ of the decay. A novel CMOS direct charge detector, Topmetal-S, was proposed for $0\nu\beta\beta$ search in a Time Project Chamber (TPC) without gas avalanche amplification. Topmetal-S utilizes a low-noise charge sensitive amplifier (CSA) to measure the charge and a high-precision $\Sigma\Delta$ ADC for digitization.

The ADC is composed of an analog $\Sigma\Delta$ modulator and a decimation filter in digital domain. Sampling the input at a frequency that is much higher than the signal bandwidth (oversampling), coupled with noise shaping of the modulator, the majority of the quantization noise power is shifted beyond the frequency band of interest. Appropriate digital filtering decimation is required to attenuate the out-of-band noise to achieve adequate signal-to-noise ratio (SNR) and to lower the bit rate for transmission and processing.

A fully differential, switched-capacitor and cascaded third-order $\Sigma\Delta$ modulator was implemented. A single-bit quantizer was chosen for its overall advantage in linearity, area, and power consumption. The first stage consists of two integrators, a comparator that serves as a 1-bit ADC, and a distributed two-level (1 bit) DAC. The second stage consists of a single integrator, a 1-bit ADC, and a 1-bit differential DAC. The modulator operates on a two-phase non-overlapping clock consisting of a sampling phase and an integration phase. Necessary dynamic range scaling is done to ensure that the outputs of all stages of the modulator remain bounded.

A four-stage cascaded integrator-comb (CIC) decimation filter was coupled to the third-order modulator. This is the simplest and most economical filter since it does not require a multiplier. The CIC filter consists of 4 sections of cascaded integrators, then a downsampler with factor of 64, followed by 4 sections of cascaded comb filters. An LVDS interface is used to drive the output data stream.

Tests show that the $\Sigma\Delta$ ADC could operate effectively as a 14-bit, 400k samples per second (SPS) waveform digitizer, consuming 39.6 mW with a single 3.3 V power supply. It satisfies the needs of a novel CMOS direct charge sensor, Topmetal-S, for $0\nu\beta\beta$ search in TPC. The main design considerations, including ADC architecture, resolution, speed, power consumption and stability, are discussed. The design of the $\Sigma\Delta$ ADC was based

on a top-down CAD methodology that combines simulation and statistical optimization at various levels of the modulator hierarchy.

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