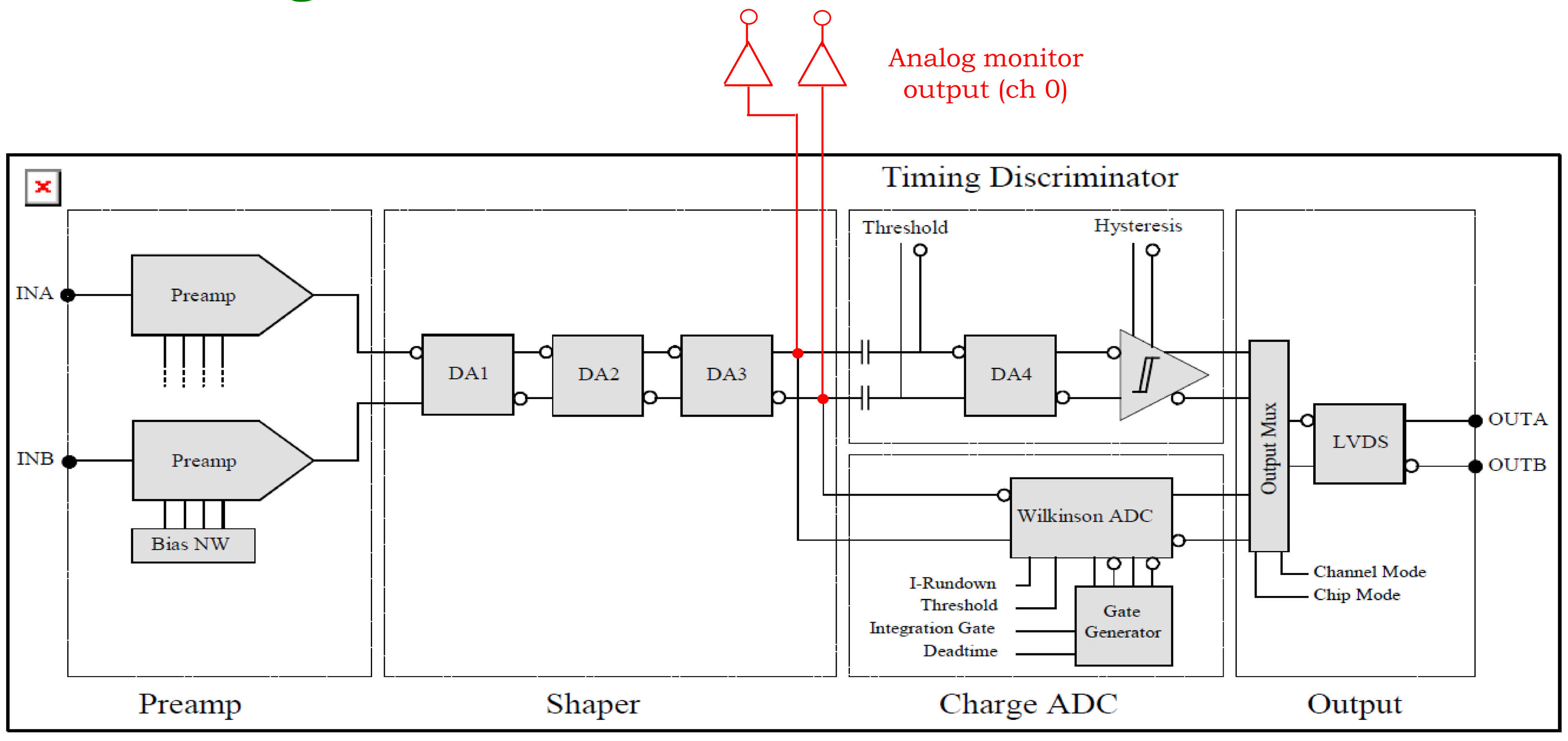
Development and performance of the new front-end ASIC for the ATLAS MDT chambers at the HL-LHC

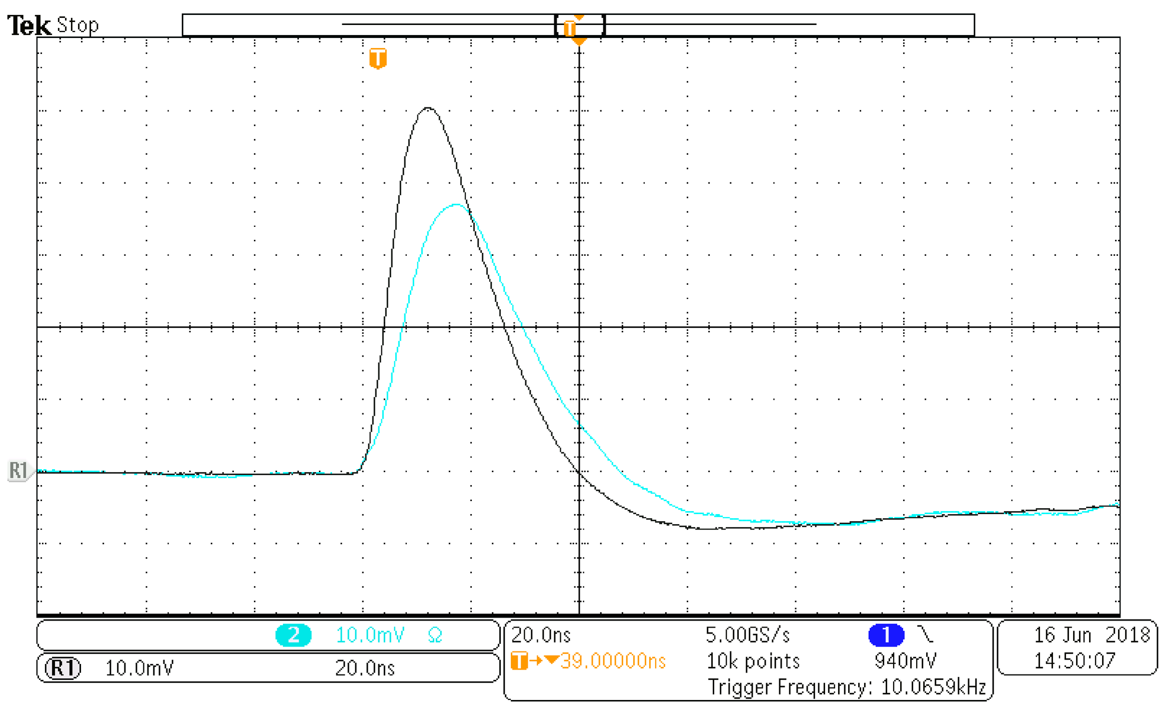
The task

Following the necessity to replace the front-end electronics of the ATLAS Monitored Drift Tube (MDT) chambers, a new MDT-ASD2 ASIC has been developed and tested. The ASD2 comes as a replacement of the original ASD and has been optimized for the MDT chamber readout in the HL-LHC environment. The ASIC is made in IBM 130nm CMOS 8RF-DM technology and provides superior chip-to-chip and channel-to-channel uniformity among functional parameters like peaking time, channel gain and matching of discriminator threshold and programmable dead-time.

Functional diagram of the ASD

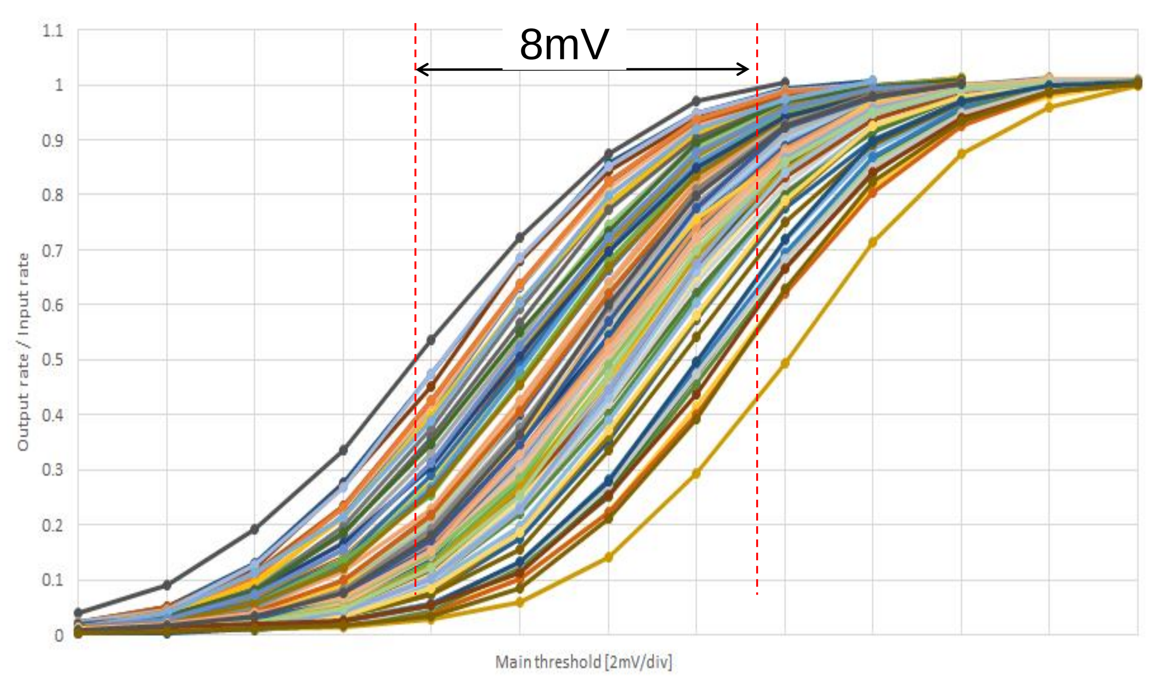


Preamp/shaper peaking time



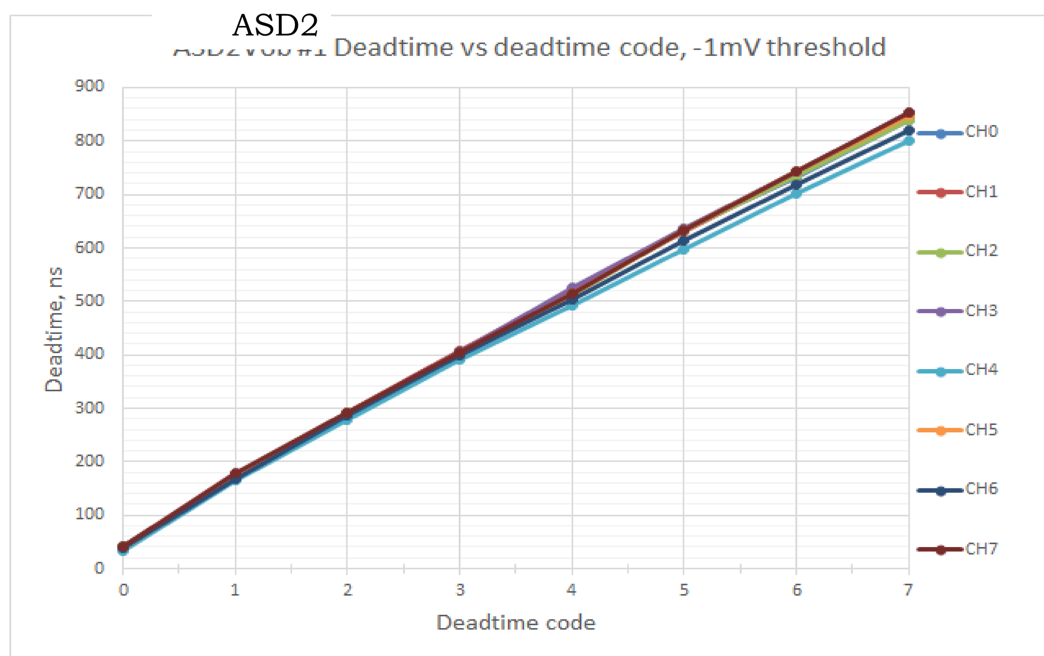
Shaper response to a 50 fC input charge. The peaking time without capacitive load (black) is 11ns. With a 60pF capacitive load (blue) it only increases to 15ns. The typical capacitive load of ATLAS MDT tubes is ~30 pF.

Channel threshold uniformity



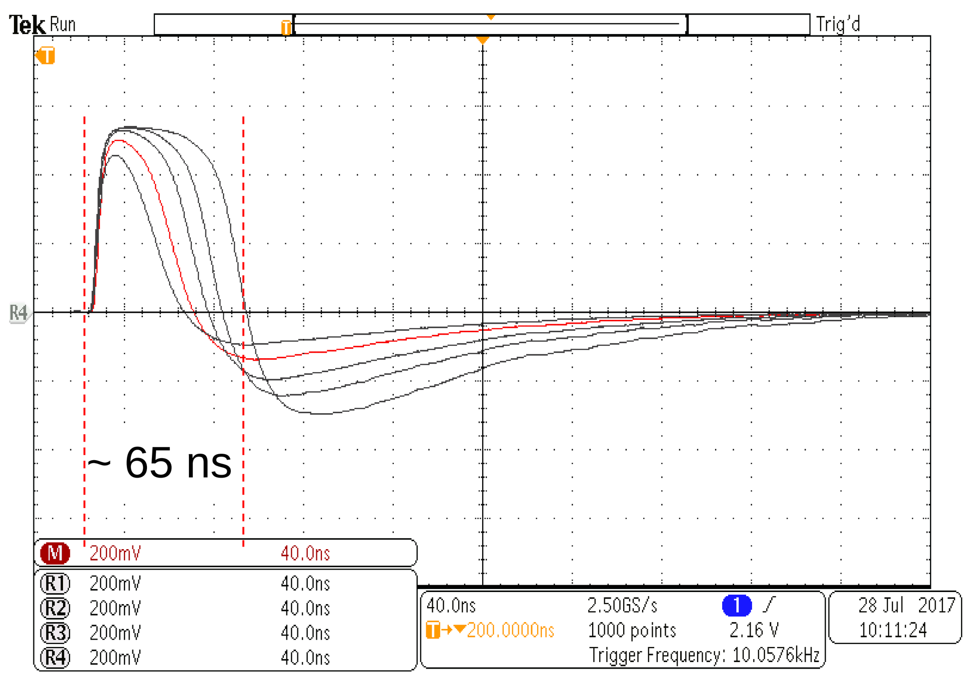
Threshold scan for 12 ASD2 chips (96 channels). The threshold variation of more than 90% of the ASD2 channels is in the range of 3-6mV.

ASD2 dead-time uniformity



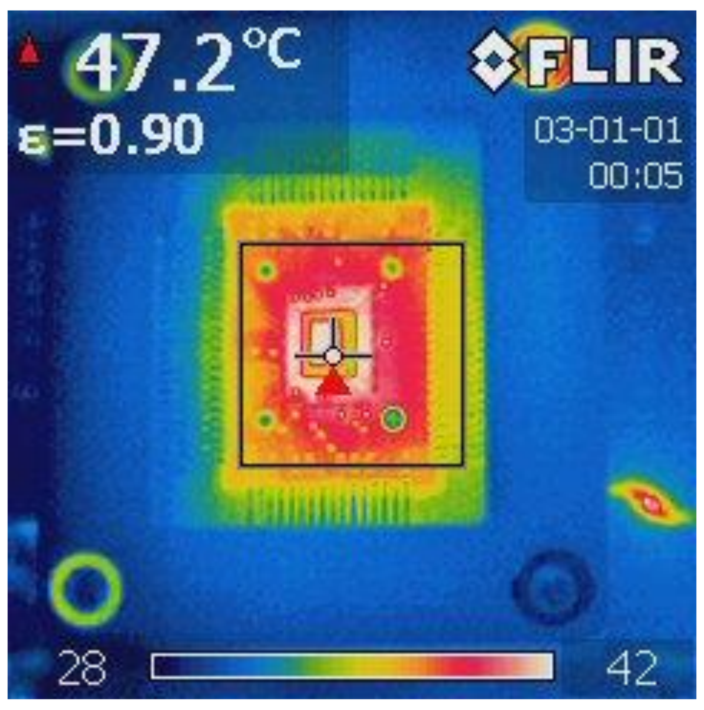
Each channel can be disabled by a programmable dead-time in the range 30-800 ns. The non-uniformity among the 8 channels of a chip and among different chips is below 4%.

Pulse shape for input overload



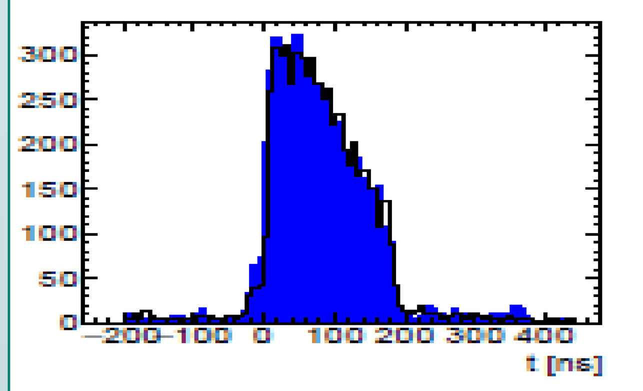
Because of the Landau fluctuation of the primary ionization, a wide range of input charges must be handled by the amplifier without excessive dead-time (baseline return). The diagram shows shaper outputs for input charges 100-2000 fC

ASD2 at V_{cc} = 3.3V

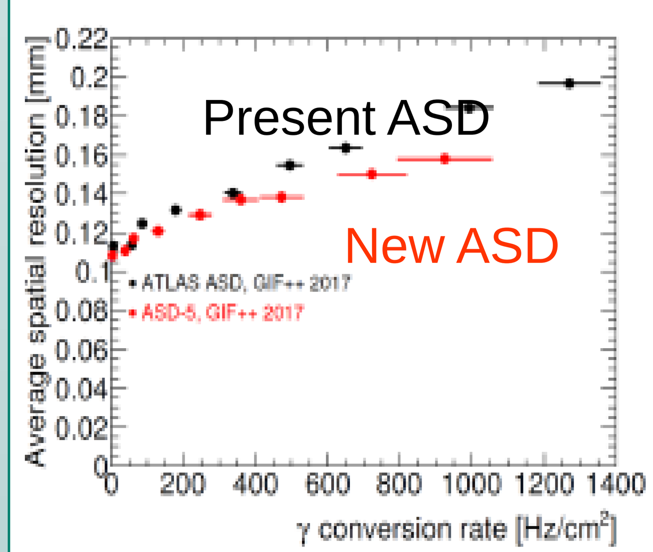


An infrared photo of an unpackaged chip, wire-bonded to a PCB. The PCB contains a solid copper layer below the chip for better heat dissipation. The steady state die temperature is at a safe value of ~47C.

Test beam results at GIF++



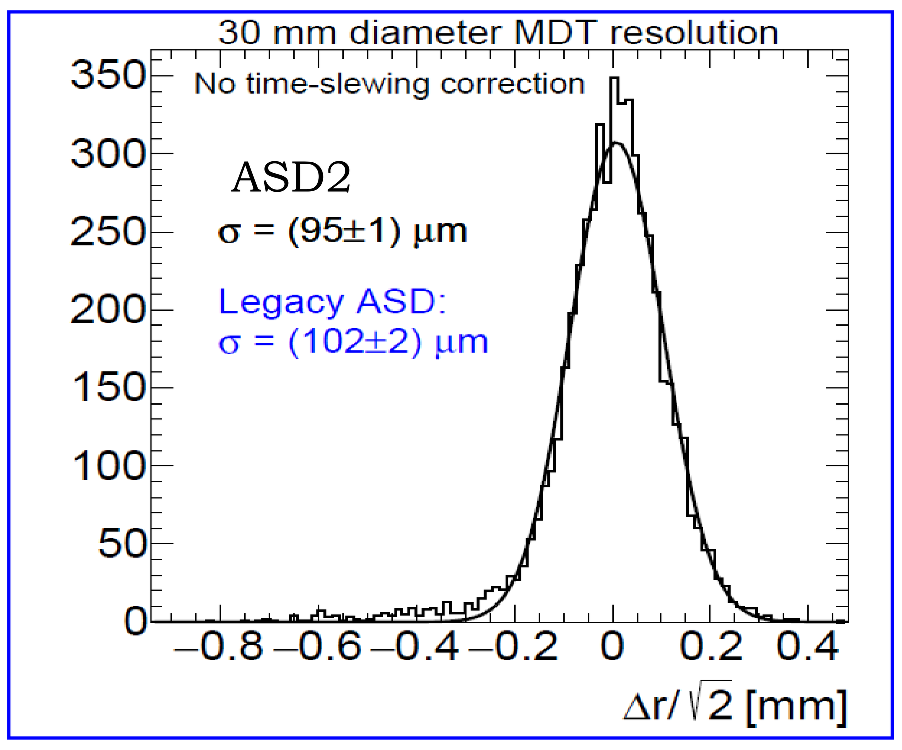
The drift time spectra with the **present ASD** and with the **ASD2** agree very well.



Average drift tube spatial resolution with **present** and **new ASD2** vs γ count rate, as measured at the GIF++ facility at CERN. Rates ***in the experiment*** are expected to be below 500 Hz/cm².

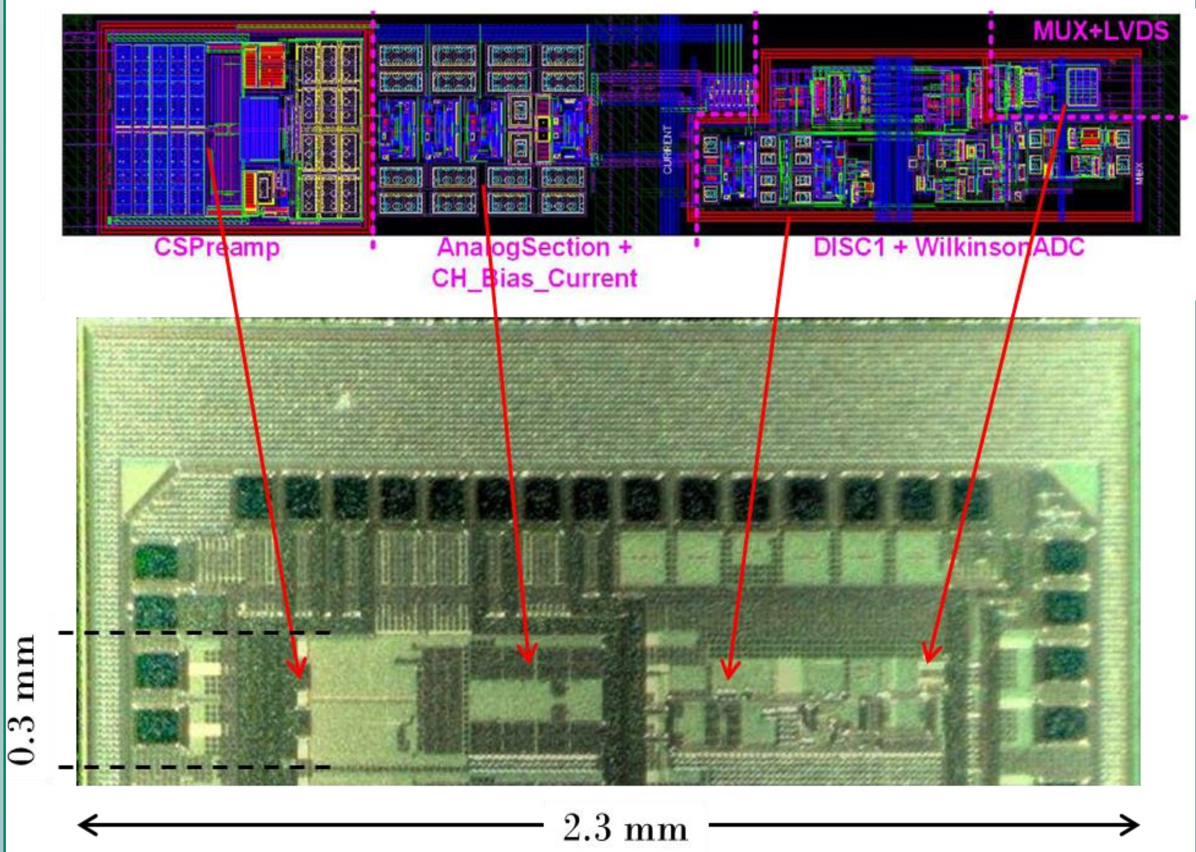
The higher gain of the new ASD reduces time-slewing and may lead to a better spatial resolution.

Spatial resolution for 150 GeV muon tracks using the New ASD2



Measurement without γ background.

Layout and photo of one channel of ASD2



Time schedule for ASD2 production and installation

2017 Last MPW run and characterization, Preliminary Design Review
2018 Successfull radiation test for TID up to 1MRad (required 20kRad)
2018 ASD2 was been approved in an ATLAS FDR for an engineering run (2 wafers with ~4k chips).
2019 Bonding, packaging & testing of 4k chips
2020 Reception of production run with 80k chips (~40 wafers); bonding, packaging; QA/QC tests
2021 Integration with TDC on a common mezzanine card
2022 Installation in the experiment

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