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Development and performance of the new front-end ASIC for the ATLAS MDT chambers at the HL-LHC

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Following the necessity to replace the front-end electronics of the ATLAS Monitored Drift Tube chambers, the new MDT-ASD2 ASIC has been developed and tested. The ASD2 comes as a replacement for the original octal Amplifier/Shaper/Discriminator optimized for the MDT-chamber readout for HL-LHC. The ASIC is made in IBM 130nm CMOS technology and provides superior chip-to-chip and channel-to-channel uniformity among functional parameters, e.g. peaking time, channel gain, discriminator threshold and channel dead-time. The paper presents the general design strategy, simulation and lab test results, off and on-chamber, as well as test beam data taken at CERN with and without gamma irradiation.

Summary

The first processing stage of an ATLAS Monitored Drift Tube (MDT) readout electronics, the Amplifier-Shaper-Discriminator (ASD), largely determines the overall performance of the MDT chambers for crucial parameters like time resolution, efficiency and noise rejection. The MDT ASD is an 8-channel amplifier-shaper-discriminator ASIC with charge-to-time converter based on a Wilkinson ADC which has a variety of programmable parameters. The ASD2 prototype design is done in the well-established and supported, radiation tolerant 130nm IBM CMOS 8RF-DM technology on the basis of original ASD design features.

The ASD provides two modes of operation - Time-Over-Threshold (ToT) and ADC mode. Each ASD channel includes an input stage, a charge sensitive preamplifier converting the input charge into a voltage, followed by 3 shaping stages, discriminator and the Wilkinson-type ADC, which is enabled depending on the operation mode. In ToT mode, the discriminator output is directly routed to the channel output pins. It reflects the crossing of the programmed threshold by the amplified and shaped signal. In the experiment, this threshold crossing determines the arrival time of the ionization charges at the sense wire of the drift tubes. But because of finite rise time and bandwidth, the threshold crossing time on the amount depends on the incoming charge and on the threshold itself. The ADC charge measurement is used to reduce this dependence in order to increase the accuracy of the time measurement (time slewing corrections).

The ASD design uses a common DAC to provide the threshold for all 8 discriminators on the chip. Great emphasis was put on minimizing channel-to-channel gain variation and internal offsets, to reduce intrinsic channel noise and crosstalk and to achieve high uniformity of the operating. The analog path was modified and made fully differential, compared to the original ASD ASIC, where the preamplifier consisted of a single-ended (i.e. common source) analog gain stage with feedback capacitor. Post-layout simulations validated this choice, demonstrating that unwanted supply noise is attenuated of -7dB at the output of the first stage.

The ASD2 ASIC occupies an area of 7.64 mm2 and has a sensitivity of about 10mV/fC, 10 ns peaking time at the discriminator input and 10 mA current consumption per channel at 3.3 V supply voltage. Tests of a large quantity of prototype chips and a full characterization of the chips have been performed. An automated chip test setup has been developed for this purpose. Post-layout simulation and laboratory test results (on- and off-chamber) show good agreement for all performance parameters. Test-beam data taken at CERN with and without gamma background irradiation show that the new ASD ASIC performs equally well or better compared to the original chip on real muon and gamma signals in a MDT chamber with respect to drift tube time and spatial resolution. An irradiation test of the new chip for gamma doses up to xxx Rad is also in

progress. After having successfully passed all tests, the production of the 60,000 ASD2 chips required for the ATLAS MDT electronics upgrade for HL-LHC is foreseen for 2019-20.

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