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Study of Time of Arrival Measurement with Constant Fraction Discrimination Using Switched Capacitor Sampling or Bucket-Brigade Analog Time Delay Line

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Time of arrival measurement using the constant discrimination technique built upon continuous switched capacitor sampling of an input waveform with a precise and high frequency clock or with a bucket-brigade-type integrated MOS analog delay line for producing a delayed version of the input signal is presented. The concepts are laid out and analyzed. The relation between the sampling or shifting time interval, degree of low pass filtering of the sampled and delayed waveform, DC-level restoration and obtainable time of arrival measurement precision as well as studies of power consumption and implementation as an integrated circuit block are reviewed.

Summary

The Phase II Upgrade of the CMS experiment includes the End-Cap Timing Layer (ETL), whose role will be to register not only positions of particle impacts, but also times when the hits are received. Timing dimension is for dealing with the expected pile-ups due to multiple collisions in the HL-LHC that result in creating primary vertices from where particles spring off to the detector layers. The ETL intends using Low-Gain-Avalanche-Photodiodes with pixelization on the order of up to a few mm square as a sensor.

Typically, the first blocks in the measurement chain are a voltage or current pulse generating circuit and a discriminator, whose role is to detect when an analog signal meets given criteria, e.g. threshold crossing or changing polarity [1]. The challenge in designing of a circuit that would be able to provide a precise time of arrival measurement irrespective of the form and amplitude of the pulse signal is twofold. First the right method of the measurements needs to be chosen and, then, its realization should be possible in an integrated circuit. The leading-edge method is simpler but it requires a clean rising edge of the signal and suffers from the signal-amplitude-dependent time-walk. On the other hand, the constant fraction discrimination (CFD) method is known to stably yield indicate when the processed signal changes it polarity, but it requires delaying of an original signal, which cannot find its pure realization in an integrated circuit. Thus, known solutions use additional low-pass filtering for obtaining the delayed version of the pulse signal, yielding a dependence on the processed signal.

This work introduces continuous switched capacitor sampling of an input waveform with a precise, low-jitter and high frequency clock [2] or with a bucket-brigade-type integrated MOS analog delay line [2] for producing a delayed version of the input signal to be used in the CFD method. Sampling on a capacitor array or progressing through the delay line is achieved using the recycled clock from the in-pixel fine delay-locked-loop used for registering events in time bins. The delayed waveform is low-pass filtered to reconstruct its smooth form and subsequently subtracted from the input signal after its scaling to form a bipolar signal that is sought for zero-crossing time. It is believed that the closest to the actual theoretical definition of the CFD time of arrival measurement method can be obtained in an integrated circuit following the presented scheme.

The paper reviews the concepts of time of arrival measurement with CFD using switched capacitor sampling or bucket-brigade analog time delay line. It discusses the relation between the sampling or shifting time interval, degree of low pass filtering of the sampled and delayed waveform, DC-level restoration and obtainable time of arrival measurement precision. Power consumption and implementation as a block in an integrated circuit

are also reviewed.

References:
1) H.Spieler, IEEE Trans. on Nuclear Sci., Vol. 29, No.3, (1982), pp. 1142-1158
2) R.A.Mao, et al., IEEE Journal of Solid State-Circuits, Vol. 4, No. 4, (1969), pp. 196-201
3) US 6,222,409 B1

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