PSEC4A : A 10 GSa/s Waveform Sampling ASIC with Multi-Event Buffering Capability

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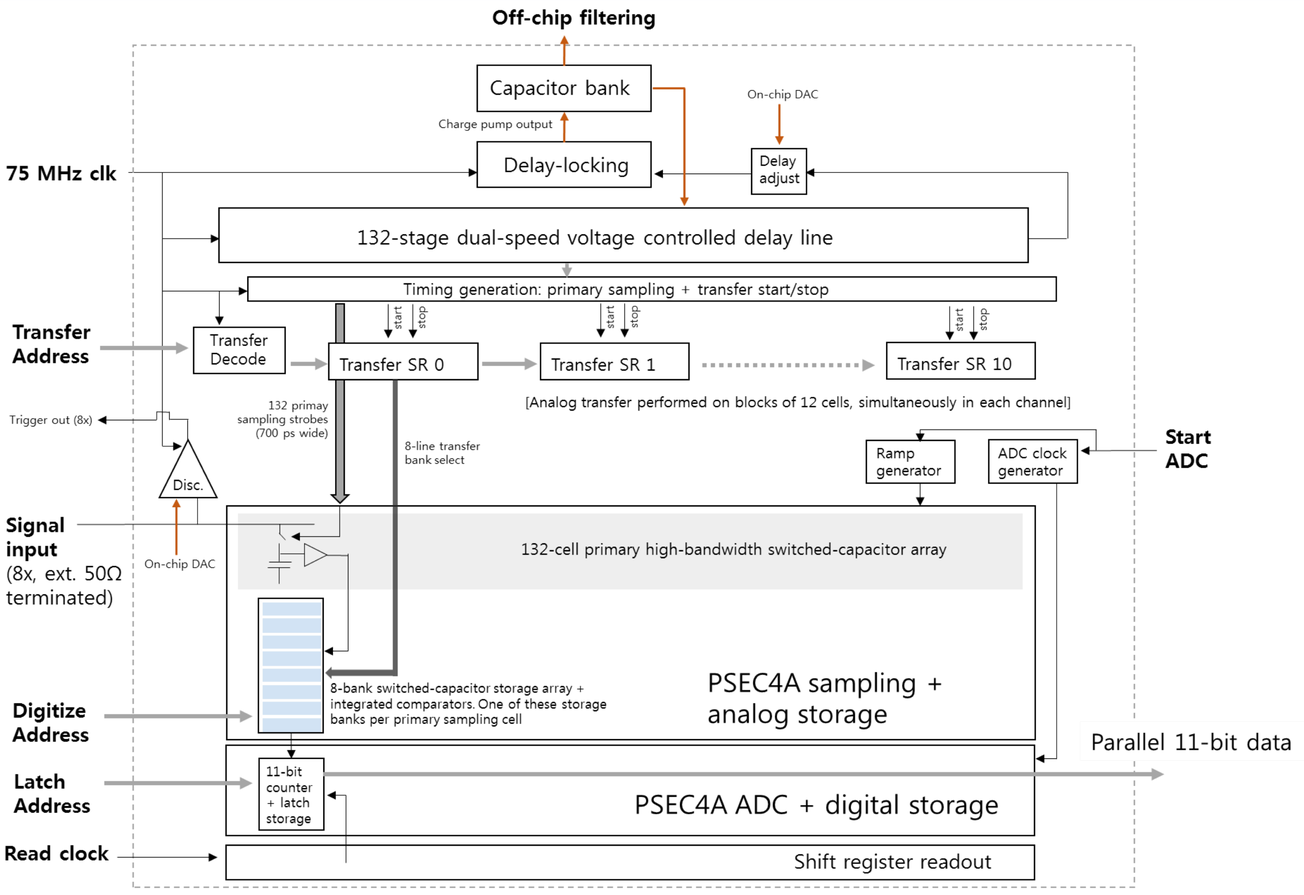
Abstract

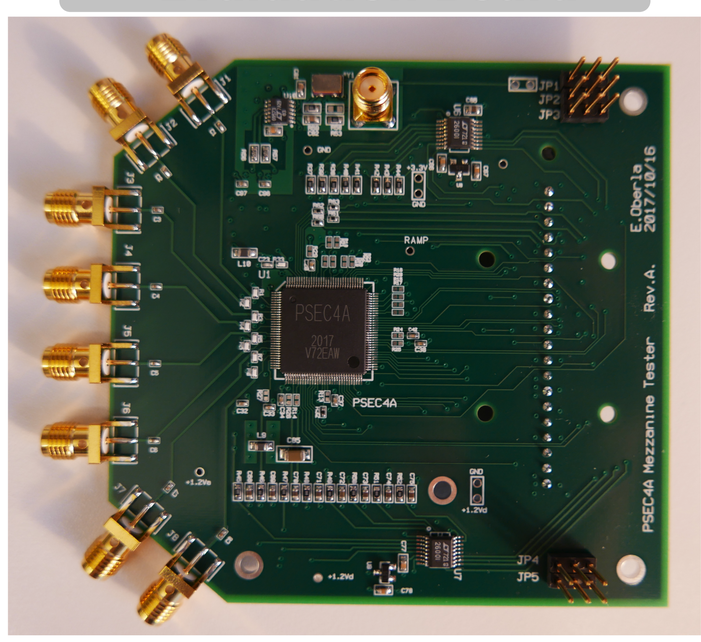
We present the design and performance of PSEC4A: an 8-channel, 10 GSa/s switched-capacitor array waveform sampling and digitizing ASIC designed in 0.13 µm CMOS based on the PSEC4 chip[1,2]. The PSEC4A incorporates multi-event buffering to reduce deadtime-induced latency for close-in-time triggers by using a primary sampling array of 132 switched-capacitors that can be written to a bank of 1056 storage capacitors, which are segmented in 8 randomly-accessible blocks. With a dual-speed voltage control delay line, the sampling rate is stable over a wide range from 1-10 Gsa/s. Each channel has an integrated 11-bit ramp-compare ADC with shift-register readout that permits simultaneous sampling, digitization, and readout operations. Single-level discriminators are included with each channel and the trigger thresholds can be set using on-chip 10-bit DACs. The ±1 dB bandwidth is 920 MHz, which is limited by the relatively long bondwires in the prototype ASIC package. The -3dB analog bandwidth is measured to be 1.9 GHz.

Chip Architecture



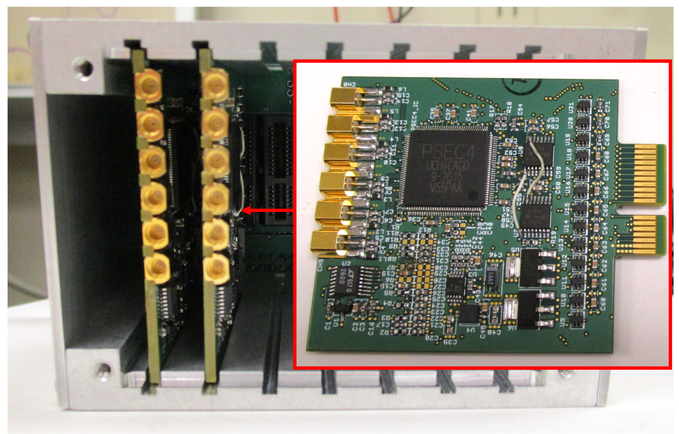
- The PSEC4A is based on a 132-sample primary switched capacitor array (SCA), which is driven by an voltage controlled delay line that feeds a timing generator circuit. At 10GSa/s operation, ~700 ps wide sampling strobes are generated for each primary cell.
- Each primary cell has a buffer amplifier and a closely integrated bank of 8 storage capacitors, which are addressable by the FPGA controller. The transfer window is hard-wired on chip to be 96-sampling intervals in duration. Blocks of 12 primary cells are transferred to the addressed storage cell simultaneously in all channels over a period of ~10 ns (when running at 10 Gsa/s).
- The PSEC4A analog-to-digital circuitry is heavily drawn from the earlier PSEC4 ASIC[1]. The ramp-compare ADC runs to 11-bit resolution on a 1 GHz ring-oscillator derived clock, taking 2 µs to finish converting 132 samples * 8 channels in parallel.
- Digitized data are stored in a 4-bit serial latch that is included with each bit in the ADC counter, which saves the digital samples before the higher latency serial readout (~2 µs per 132 samples per channel). This permits rapid digitization of 528 samples on all channels (finished in ~8 µs) to prevent any significant sample degradation from leakage on the primary SCA.
- Timing of `wraparound' interval (sample 132→1) can be tuned with an on-chip delay to remove gaps in sampling

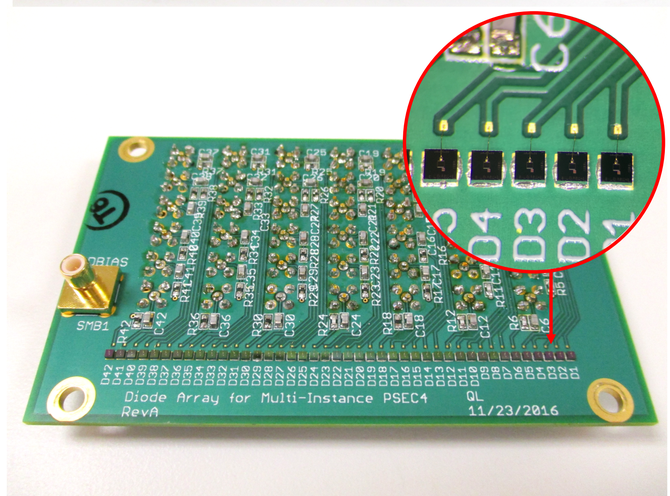
Evaluation Board



- The PSEC4A is packaged in a 128-pin LQFP package. This is oversized for the 4x4 mm^2 die, but allowed the monitoring of a number of debugging signals and all of the internal DAC values (which have been verified as functional).
- The internal DACs and other settings are programmed using a serial interface within the chip
- This mezzanine board plugs into a FPGA + USB motherboard that was designed for the PSEC4 ASIC evaluation.
- The board uses a 75 MHz oscillator (for a default 10 GSa/s operation), but also accepts an external clock to rapidly test other sampling rates
- The chip operates on a single +1.2V supply
- Our baseline testbench runs PSEC4A in a 528-sample `ping-pong' mode → 50 ns/waveform @ 10 GSa/s

42-Channel System



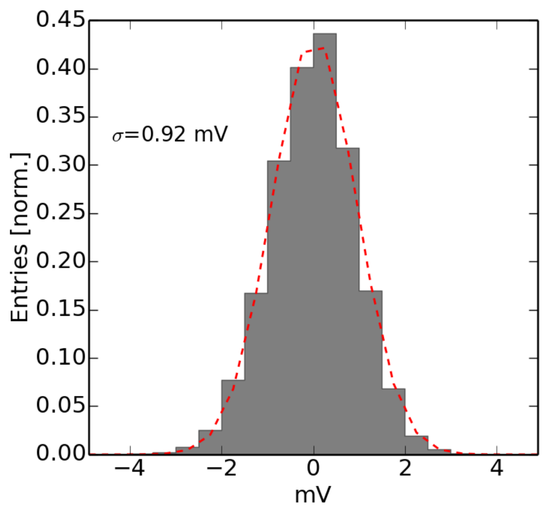


- Modular evaluation system for use as x-ray and particle detector at Sandia's Z Pulsed Power Facility[3]
- Mating 42 channel photodiode board allows customization of detectors for different applications

PSEC4A Performance

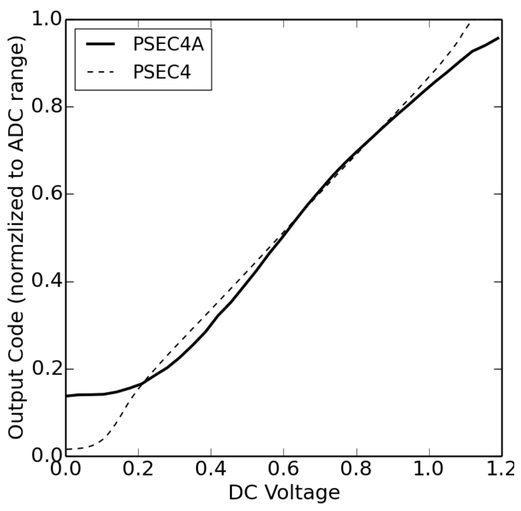
Noise

Somewhat higher than PSEC4 (0.7 mV RMS), LSB of on-chip ADC is ~0.35mV. A dominant noise source is the primary sampling capacitor (~18 fF)



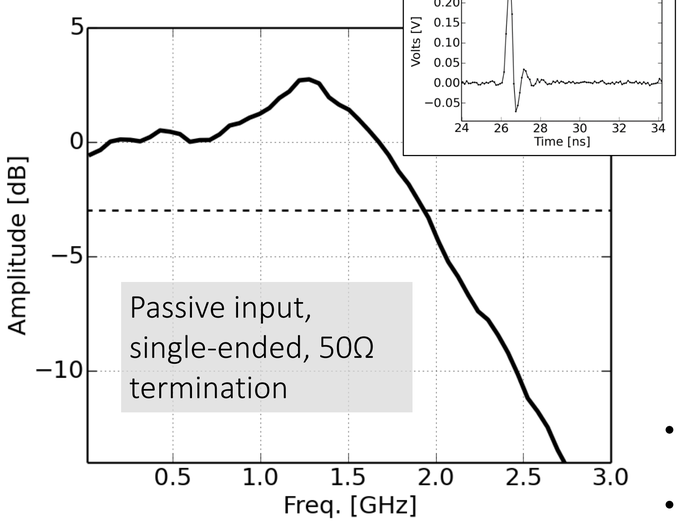
Signal Range

PSEC4A has ~0.8 V usable range on the 1.2V core voltage. The linearity performance of the ADC is poorer than the PSEC4 (<0.2% linearity deviation over a 0.75 V range) due to single-stage ADC comparator, required for compactness. It is corrected in a count-to-voltage LUT.



Analog bandwidth

Long package bondwires contribute to peaking at >1 GHz. -3dB bandwidth is measured at 1.9 GHz using an ultra-wideband impulse →



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References
[1] E. Oberla, et al. `A 15 GSa/s, 1.5 GHz Bandwidth Waveform Digitizing ASIC', NIM A735, 2014
[2] M. Bogdan, et al. `A modular data acquisition system using the 10 GSa/s PSEC4 Waveform Recording Chip', IEEE Real Time, 2016
[3] Y. Opachich, et. al. 'Solid State Streak Camera Prototype Electronic Performance Testing and Characterization', Proc. SPIE, 10390, 103900L (2017)

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