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A 10 GSa/s Waveform Sampling ASIC with Multi-Event Buffering Capability

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We present the design and performance of PSEC4A: an 8-channel, 10 GSa/s switched-capacitor array waveform sampling and digitizing ASIC, which incorporates multi-event buffering to reduce deadtime induced latency for close-in-time triggers. The PSEC4A chip uses a primary sampling array of 132 sampling capacitors that can be written to a bank of 1056 storage capacitors segmented in 8 randomly accessible blocks. Each channel has an integrated 11-bit ramp-compare ADC with shift-register readout that permits simultaneous sampling and readout operations. The relatively short primary sampling array allows an analog bandwidth of the input greater than 1.5 GHz.

Summary

The PSEC4A ASIC was designed and fabricated in 2017 as an upgrade to the PSEC4 waveform sampling chip. The PSEC4 offers 10 GSa/s sampling rates, self-triggering, and high bandwidth, but its applicability is limited due to a short 256-sample recording length on each channel. To address this issue, PSEC4A combines the PSEC4 digital circuitry with a new analog design, which allows a larger recording window as well as the option for multi-event partitioning of the analog buffer.

The PSEC4A has a maximum trigger latency of 100 ns at 10 GSa/s operation when using the full 1056 samples per event. Alternatively, PSEC4A may operate in multi-event buffering mode in which a subset of the 1056 samples are used per event. In this mode, PSEC4A can hold a self-triggered event for several microseconds while waiting for a global system trigger to initiate digitization and readout while keeping other subsets of the analog buffer available for capturing events from coincidental triggers. In this way, PSEC4A may be implemented as a deadtimeless readout in a particle physics detector (up to some high trigger rate).

The PSEC4A architecture utilizes a two-stage switch capacitor array: a primary sampling array that is targeted for high bandwidth and a second stage that is for long-term (˜10-100 microsecond) storage. A single-transistor buffer amplifier is used to isolate and drive the second stage. The primary sampling array is passively coupled to the input signal line and its switches are toggled with a voltage-controlled delay line (VCDL). The VCDL is common to all channels and can operate in two speed modes that allow a wide 1-11 GSa/s sampling rate range.

Analog-to-digital conversion is done on-chip using a ramp-compare ADC and a 1 GHz ring-oscillator derived clock. The ADC and single 132-sample block readout takes ˜4.5 microseconds. During this time, another event may be recorded in a different analog block, thus reducing the chip deadtime. Each channel includes a trigger discriminator and DAC for setting the threshold.

A PSEC4A 8-channel evaluation board was fabricated and is being used for performance characterization.

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