# New LpGBT-FPGA IP: Simulation model and first implementation

**J. Mendez**, S. Baron, J. Fonseca, S. Kulis

*EP-ESE-BE Section, CERN, 1211 Geneva, Switzerland*

## Abstract

High speed links are commonly used in High Energy Physics experiments for data acquisition, trigger and timing distribution. For this reason, a radiation-hard link is being developed in order to match the increasing bandwidth demand of the backend electronics and computing systems. In this framework, the LpGBT -which is the evolution of the GBTx ASIC- is being designed and is foreseen to be used by CMS and ATLAS for their Phase-II upgrades. The LpGBT-FPGA IP core is proposed to offer a backend counterpart of the LpGBT. This paper presents the status of its development, the IP architecture and the future steps.

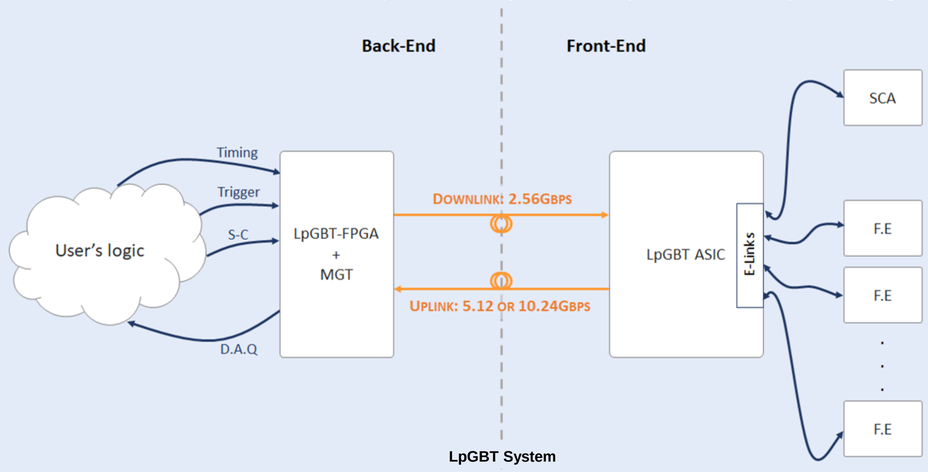
## Introduction to the LpGBT

The LpGBT ASIC (Low Power GigaBit Transceiver) is a new 65nm-CMOS radiation tolerant serializer/deserializer device that can be used to implement multipurpose high speed bidirectional links for front-end electronics of high-energy physics experiments. It targets Phase-II upgrades of the HL-LHC detectors, and in particular CMS and ATLAS. The LpGBT ASIC offers a set of encoding and decoding schemes specifically tailored to meet their needs in terms of radiation-hardness, data bandwidth and power consumption. Like its predecessor, the LpGBT is targeted to be used for three distinct features that are Timing and Trigger Control (TTC), Data Acquisition (DAQ) and Slow Control (SC).

The new LpGBT features an asymmetric architecture: a single FEC solution and a unique data rate for the downlink path (from Back-end to Front-end) and various encoding/decoding schemes and speeds for the uplink path (from Front-end to Back-end). The upstream link can be configured with 4 different combinations: two Forward Error Correction schemes (FEC5 or FEC12) based on Reed-Solomon techniques to tune the robustness of the link, and two line rates (10.24 or 5.12Gbps) set according to the required bandwidth. The receiver part of the ASIC, as opposed to its configurable transceiver part, proposes a single encoding scheme (FEC12) and a lower line rate of 2.56Gbps. In both directions, the frame itself is split into several fields: header, FEC bits but also Data and two control fields, one to configure the LpGBT itself (Internal Control, IC) and the second one to control a potential GBT-SCA through the LpGBT (External Control, EC).

| | Configuration | | User bandwidth | | | Robustness |
|---|---|---|---|---|---|---|
| | FEC Scheme | Data rate | Internal Control (IC) | External Control (EC) | Data | Max of consecutive errors corrected by the FEC |
| **Downlink** | FEC12 | 2.56Gbps | 80Mbps | 80Mbps | 1.28Gbps | 12 |
| **Uplink** | FEC5 | 5.12Gbps | 80Mbps | 80Mbps | 4.48Gbps | 5 |
| | FEC5 | 10.24Gbps | 80Mbps | 80Mbps | 8.96Gbps | 10 |
| | FEC12 | 5.12Gbps | 80Mbps | 80Mbps | 3.84Gbps | 12 |
| | FEC12 | 10.24Gbps | 80Mbps | 80Mbps | 7.68Gbps | 24 |

**LpGBT ASIC bandwidth and robustness depending on configuration**

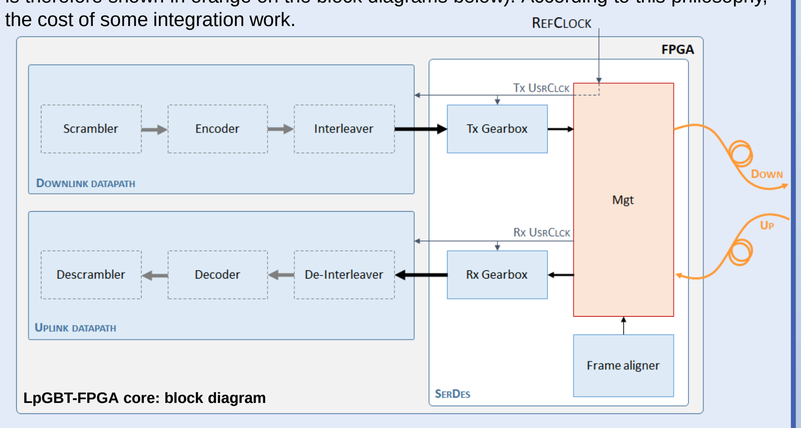



## LpGBT-FPGA: Architecture and Philosophy

As a Back-end counterpart of the LpGBT, the new LpGBT-FPGA IP mirrors the encoding/decoding schemes supported by the front-end ASIC: its transmitter only proposes one single configuration, whereas its receiver can be configured using the four combinations proposed for the upstream link as described above. **Such an asymmetry of the LpGBT-FPGA prevents the IP to be used in loopback mode for self-testing**.
In a view of simplification, the LpGBT-FPGA core is exclusively made of a set of generic VHDL modules (displayed as light blue boxes in the diagrams) which can be configured in order to match the user's choice and the LpGBT configuration. For example, the uplink datapath can be set to any FEC/rate combination. This new paradigm also implies that **the MGT (Multi Gigabit Transceiver) of the FPGA is not anymore part of the LpGBT-FPGA core itself**, as opposed to the former GBT-FPGA core (the MGT block is therefore shown in orange on the block diagrams below). According to this philosophy, resources and performance can be fully optimized by the user, at the cost of some integration work.

In order to guide the user in this task, the LpGBT-FPGA core is now proposed as a set of modules with implementation examples and reference notes:

- **The Datapath modules**: Contains the logic required for data scrambling, encoding, interleaving in one hand, and for the de-interleaving, decoding and descrambling in the other hand. Both FEC (FEC5 and FEC12) schemes are available and selectable for the Uplink path. The two top entities can be configured for dynamic or static modes.
- **The Gearbox modules**: Used to convert the LpGBT frame into MGT word, and vice-versa. They are fully configurable depending on the the MGT configuration and guaranty a proper clock-domain crossing (based on multi-cycle paths) if required.
- **The Frame aligner**: Responsible for the frame alignment on the Rx side using the header.

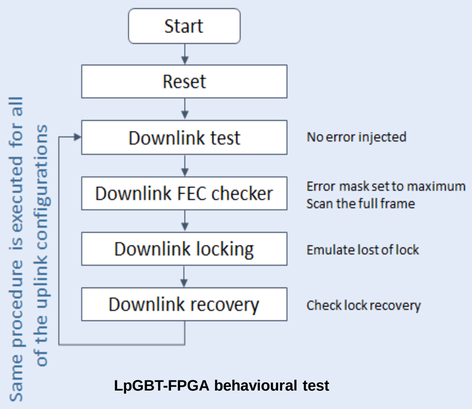



**LpGBT-FPGA core: block diagram**

It is finally worth noting that the LpGBT-FPGA logic now runs at **one unique frequency**, which shall be a multiple of the LHC Bunch Clock frequency also synchronising the MGT reference clock and the MGT user clocks.

## Status and future plans

The first version of the LpGBT-FPGA was released in July 2018. It came with a simulation test bench, used in QuestaSim. The first hardware test bench was developed and has just been released.



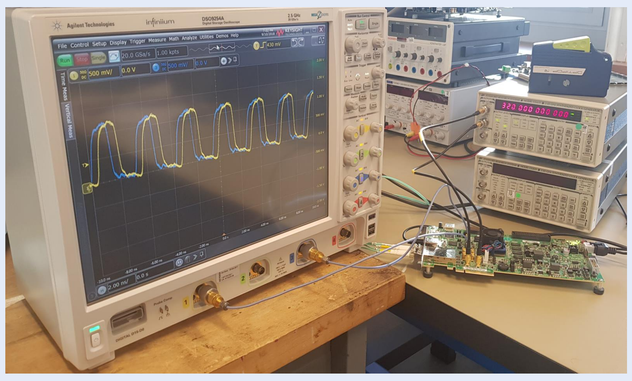

**LpGBT-FPGA behavioural test**

Continuous integration tools, supported in GitLAB at CERN, provide a way to automatically run the simulation every time a new version of the IP is pushed. Therefore, a script was designed to automatically check the core functionality, and especially the correction capability of the modules. The algorithm presented on the left describes the procedure systematically used to check the LpGBT-FPGA core behavior at every push.

Once the core had been successfully validated using this model, a new test bench targeting the KCU105 development kit from Xilinx was designed to check the timing aspect and carry out some tests with real transceivers and optical fibers. A first bunch of tests, consisting of data integrity checking and latency monitoring, was carried out. A deeper series of measurements is planned to be performed upon LpGBT prototypes delivery. The photo below shows the setup used to validate the design.

After having ensured a successful compilation and timing-closure of the design targeting the Xilinx Kintex Ultrascale FPGA, additional modules were added for the LpGBT-FPGA control and monitoring. They mainly consist of ILAs, VIOs and a JTAG-To-Axi controller in order to perform automatic resets, to check the locking state and to measure the downlink latency.

These control and monitoring modules were used to perform a first latency measurement with the LpGBT emulator (a simplified synthesizable version of the LpGBT serdes). This result will certainly change with the final component but the first result is encouraging with a downlink latency of 155ns and a stability between Tx and Rx clocks, using the HPTD module, of 12ps.

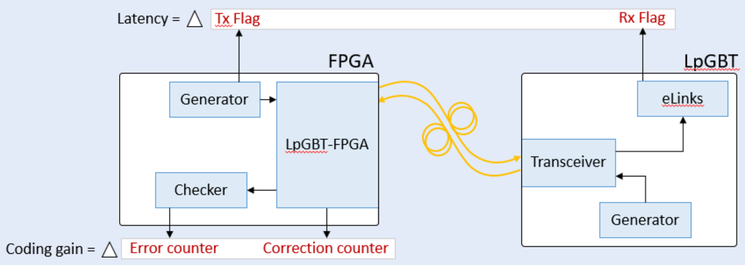


**LpGBT-FPGA Hardware test**

The IP modules and the test benches can be downloaded from the GIT repositories listed below.

- **LpGBT-FPGA IP**: https://gitlab.cern.ch/gbt-fpga/lpgbt-fpga
- **Simulation test bench**: https://gitlab.cern.ch/gbt-fpga/lbgbt-fpga-simulation
- **KCU105 test bench**: https://gitlab.cern.ch/gbt-fpga/lpgbt-fpga-kcu105

Upon reception of the first LpGBT ASICs, expected by the end of the year, additional tests will be performed to measure the frame latency and its variation on the downlink path as well as the coding gain on the upstream link.




**Test setup planned to be used for the LpGBT-FPGA qualification**

Latency measurements will be carried out using a pattern generator and an e-link output. The upstream coding gain will be measured using the internal error corrected counter from the LpGBT-FPGA, the data checker and the data generator integrated into the ASIC.

In a second phase, an additional test will be carried out to measure the downlink coding gain based on the PRBS checker and the error corrected counter modules integrated into the front-end component.

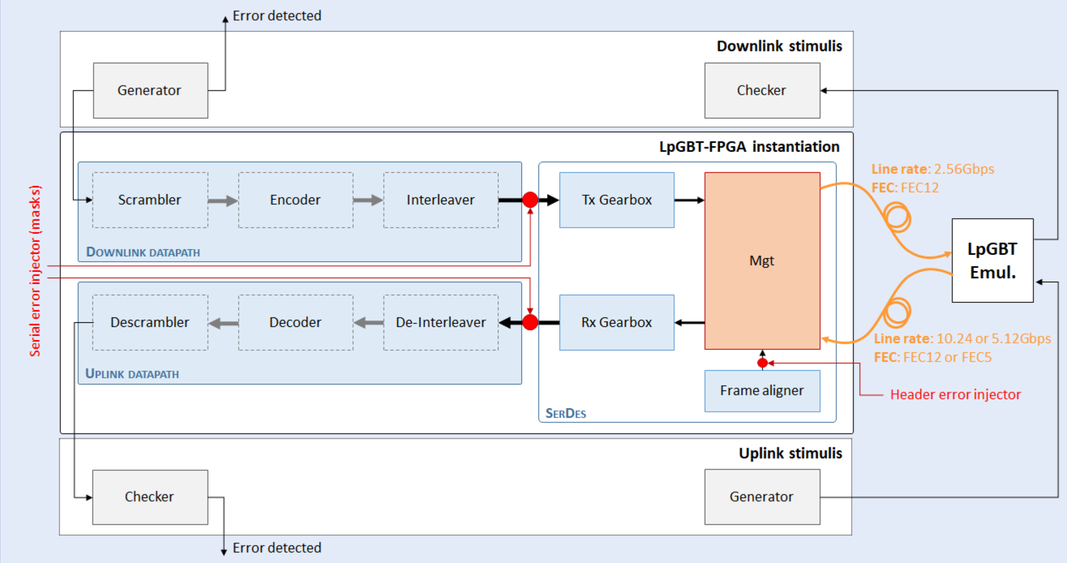
These measurements are planned to be done using the first validated prototypes (LpGBT and VTRx+).

Finally, the next step will consist in the development of a slow control module to handle the Internal control field and the integration of the GBT-SC IP to communicate with the SCA.

## Test benches: Simulation and Example design

As opposed to the GBT-FPGA project, no example designs are included into the main LpGBT-FPGA repository. However, two test benches are made available as independent projects: one as a simulation testbench, the other one as an hardware implementation (for KCU105). They shall not be re-used as is in complex designs, but more considered as examples of implementation, or as test platforms to check the functionality and measure the performance. Therefore, these models are not supported in a sense that the entities of the VHDL blocks as well as the logic can be modified anytime by the LpGBT-FPGA team to implement additional test features or to strengthen the tests.

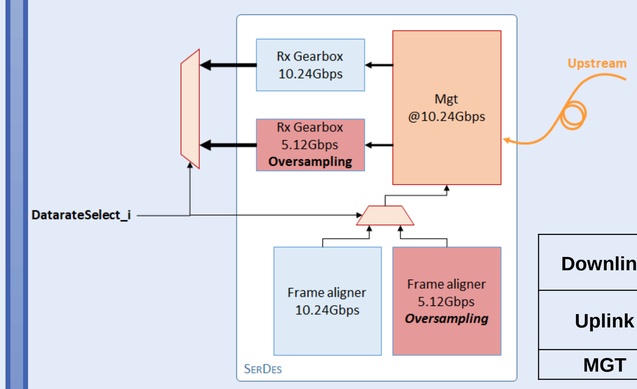
The architecture of the two test benches is identical. Because the front-end chip is not yet available, a part of the LpGBT ASIC's logic dedicated to SERDES functions is used to emulate the front-end encoding/decoding functions and is implemented as a "LpGBT Emulator". The LpGBT-FGPA core (in blue) is complemented with a MGT (in orange) and surrounded with pattern generator/checkers (in grey) and error injectors to simulate data corruption similar to the expected failures caused by SEUs in high-energy physics experiments (burst). The only difference between the hardware implementation and the simulation is the MGT module: the simulation is based on a simple emulation of a transceiver when the KCU105 design uses the Xilinx GTH IP. The block diagram below shows the test platform environment.




**LpGBT-FPGA Test benches architecture**

As the LpGBT-FPGA core (in light blue) is based on VHDL generic entities, it is not foreseen to provide a complete example per existing platform, but rather to focus on the transceiver instantiation, offering release notes describing the minimal configuration required to implement the LpGBT-FPGA IP into each FPGA.

Still, in order to propose test benches generic enough to test all of the uplink configurations, the LpGBT-FPGA features a 'dynamic mode' instantiating all the FEC and Data rate modes. This avoids compiling the design for each case and allows dynamic reconfiguration of the FEC/rate for testing purpose. However, this is not recommended for final design as it duplicates the logic as shown in the block diagram below. When the IP is implemented to run at a specific speed ('static mode'), only one Rx gearbox and one frame aligner are required. Additionally, the MGT can be specifically targeted to work at the selected data rate.




**SerDes implementation in dynamic mode**

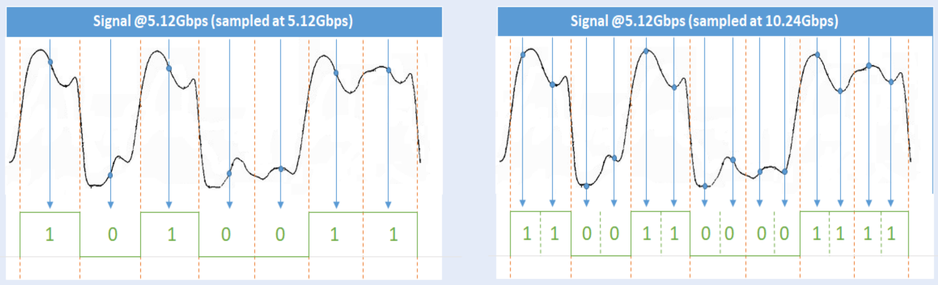
When the rate is set in dynamic mode, the MGT has to be configured for 10.24Gbps. Some logic duplication is also done in the data path in order to allow selecting dynamically the decoding scheme (FEC5 or FEC12) in dynamic FEC mode. The table below shows the resource usage for the configuration selected for the KCU105 test bench.

| | | Resource usage | |
|---|---|---|---|
| | | LUT | KCU105 |
| **Downlink** | Data path | 100 | 0.04% |
| | SerDes * | 150 | 0.06% |
| **Uplink** | Data path | 2348 | 0.97% |
| | SerDes * | 551 | 0.23% |
| **MGT** | Transceiver | 186 | 0.07% |

* Includes gearboxes and frame aligners

**KCU105 resource usage**

The logic duplication is not the unique penalty of the dynamic data rate mode. Indeed, the 5.12Gbps line rate forces the transceiver (configured at 10.24 Gbps) to oversample each bit by a factor two, meaning that each bit cannot be sampled in the center of the UI, where the best quality is expected (see pictures below). Once the final mode of the LpGBT ASIC has been selected, it is recommended to implement only the requested mode and configure the MGT accordingly.




**LpGBT-FPGA in dynamic data rate mode: oversampling penalty**

## Conclusions

The LpGBT-FPGA core is now ready to be used. A simulation test bench (based on a simplified LpGBT model) is available for behavioral analysis. In addition, a hardware testbench (based on KCU105 from Xilinx) has just been released for further testing and characterization. Because of the LpGBT component complexity (multiple FEC and datarate, up/down asymmetry, …), the FPGA counterpart is not anymore provided as a complete core but is available as a set of generic VHDL modules coming with a detailed documentation (http://lpgbt-fpga.web.cern.ch). The integration task is therefore let to the user, in particular the connection of the IP to the MGT. During the coming months, the GBT-FPGA team, in collaboration with LpGBT designers, will focus on simulating the system with the final model of the component and prepare a test setup to perform a full LpGBT-FPGA qualification.

**Contact us**: GBT-FPGA-support@cern.ch

TWEPP, Antwerpen, 17 – 21 September 2018