Introduction to the LpGBT

The LpGBT architecture is a Low-Power Gigabit Transceiver, which offers a low-power, low-latency, and high-speed solution for data transmission. It is part of the LpGBT framework and is designed to support multiple protocols and data rates. The LpGBT architecture is designed to support various protocols, including Gigabit Ethernet (GbE), Fiber Channel (FC), and other high-speed protocols.

The LpGBT architecture consists of several key components, including the transmitter and receiver, a clock recovery unit, and a data-link layer protocol. The transmitter and receiver are designed to support multiple data rates, with support for data rates of up to 80Mbps. The clock recovery unit is designed to recover the clock signal from the transmitted data, allowing for accurate time synchronization.

The data-link layer protocol is designed to support various link-layer protocols, including Ethernet and Fibre Channel. This allows the LpGBT architecture to be used in a variety of applications, including network infrastructure, storage systems, and other data transmission systems.

Test benches: Simulation and Example design

As opposed to the GBT-FPGA project, no example designs were included into the main LpGBT-FPGA repository. However, two test benches are made available as independent projects: one as a simulation testbed, the other one as an hardware implementation (for KCU105). They shall not be used as is in complex designs, but can be considered as examples of implementation, or as test platforms to check the functionality and measure the performance. Therefore, these models are not supported in a sense that the entities of the VHDs (transmitter, receiver) can be modified anymore by the LpGBT-FPGA team to implement additional test features or to strengthen the tests.

The architecture of the two test benches is identical. Because the front-end chip is not available, a part of the LpGBT ASIC's logic dedicated to SERDES functions is used to emulate the front-end encoding/decoding functions and is fully synthesizable VHDL. The back-end chip is implemented as a single entity that emulates the LpGBT ASIC receiving the data and communicating with the FPGA. The simple target is an FPGA without any complex features, allowing for easy testing.

The test bench is designed to operate in a simple mode, simulating a single stimulus of a testbench for the KCU105 design the block diagram shows the test platform environment.