

## New LpGBT-FPGA IP: Simulation model and first implementation

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High-speed links are commonly used in High Energy Physics experiments for data acquisition, trigger and timing distribution. For this reason, a radiation-hard link is being developed in order to match the increasing bandwidth demand of the backend electronics and computing systems. In this framework, the LpGBT - which is the evolution of the GBTx SERDES - is being designed and is foreseen to be installed in CMS and ATLAS for Phase-2 upgrades. The LpGBT-FPGA IP core is proposed to offer a backend counterpart of the LpGBT. This paper presents the IP architecture, the status of its development and future steps.

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## 1. Introduction: the LpGBT ASIC

The LpGBT ASIC [1] (Low Power GigaBit Transceiver) is a new 65nm-CMOS radiation tolerant serializer/deserializer device that can be used to implement multipurpose high-speed bidirectional links for front-end electronics of high-energy physics experiments. It targets Phase-II upgrades of the HL-LHC detectors, and in particular CMS and ATLAS. The LpGBT ASIC offers a set of encoding and decoding schemes specifically tailored to meet their needs in terms of radiation-hardness, data bandwidth and power consumption. Like its predecessor (GBTx), the LpGBT targets three distinct features that are Timing and Trigger Control (TTC), Data Acquisition (DAQ) and Slow Control (SC).

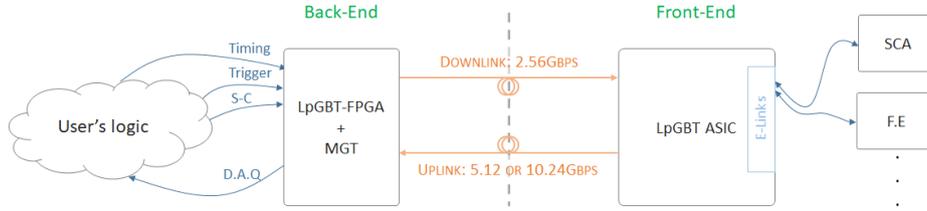


Figure 1: The LpGBT System

The new LpGBT features an asymmetric architecture: a single FEC (Forward Error Correction) solution and a unique data rate for the downlink path (from back-end to front-end) and various FEC schemes and speeds for the uplink path (from front-end to back-end) as shown in the table 1 below. In both directions, the frame itself is split into several fields: header, FEC bits but also Data and two control fields, one to configure the LpGBT itself (Internal Control, IC) and the second one to control a potential GBT-SCA or another LpGBT in slave mode through the LpGBT master (External Control, EC).

	Configuration		User bandwidth			Robustness
	FEC Scheme	Data rate	Internal Control (IC)	External Control (EC)	Data	Maximum consecutive errors corrected by the FEC
<b>Downlink</b>	FEC12	2.56Gbps	80Mbps	80Mbps	1.28Gbps	12
<b>Uplink</b>	FEC5	5.12Gbps	80Mbps	80Mbps	4.48Gbps	5
	FEC5	10.24Gbps	80Mbps	80Mbps	8.96Gbps	10
	FEC12	5.12Gbps	80Mbps	80Mbps	3.84Gbps	12
	FEC12	10.24Gbps	80Mbps	80Mbps	7.86Gbps	24

Table 1: LpGBT ASIC bandwidth and robustness depending on configuration

## 2. The LpGBT-FPGA IP: Architecture and philosophy

As a back-end counterpart of the LpGBT, the new LpGBT-FPGA IP mirrors the encoding/decoding schemes supported by the front-end ASIC: its transmitter only proposes one single configuration, whereas its receiver can be configured using the four combinations proposed for the upstream link as described above. Such an asymmetry of the LpGBT-FPGA prevents the IP to be used in loopback mode for self-testing.

In a view of simplification, the LpGBT-FPGA core, illustrated in Figure 2, is exclusively made of generic VHDL modules (displayed as light blue boxes in the diagrams) which can be configured in order to match the user's choice and the LpGBT configuration. For example, the uplink datapath can be set to any of the FEC/rate combinations presented above. This new paradigm also implies that the MGT (Multi Gigabit Transceiver) of the FPGA is not anymore part

of the LpGBT-FPGA core itself, as opposed to the former GBT-FPGA core (the MGT block is therefore shown in orange on the block diagrams below).

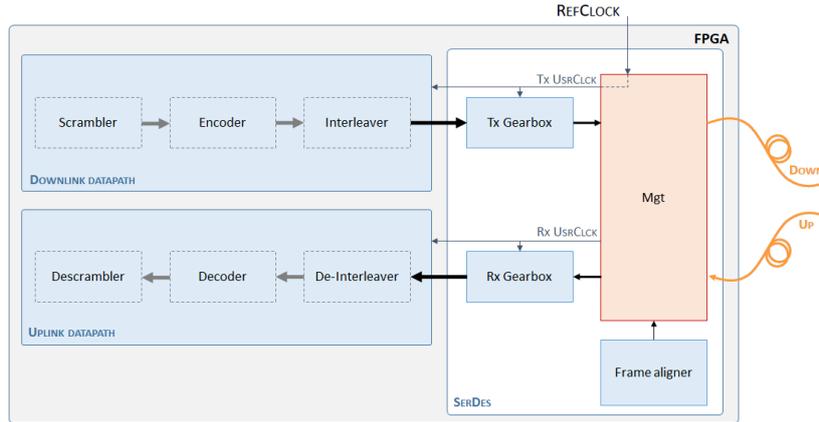


Figure 2: LpGBT-FPGA core: block diagram

According to this philosophy, resources and performance can be fully optimized by the user, at the cost of some integration work. In order to guide the user in this task, the LpGBT-FPGA core is now proposed as a set of modules with implementation examples and reference notes:

- **The Datapath modules:** Contain the logic required for data scrambling, encoding, interleaving in one hand, and for the de-interleaving, decoding and descrambling in the other hand. Both FEC (FEC5 and FEC12) schemes are available and selectable for the Uplink path. The two top entities can be configured for dynamic or static modes (see section 3).
- **The Gearbox modules:** Used to convert the LpGBT frame into MGT words, and vice-versa. They are fully configurable depending on the the MGT configuration and guarantee a proper clock-domain crossing (based on multi-cycle paths) if required.
- **The Frame aligner:** Responsible for the frame alignment on the Rx side using the header.

It is finally worth noting that the LpGBT-FPGA logic now runs at one unique frequency, which shall be a multiple of the LHC Bunch Clock frequency also synchronizing the MGT reference clock and the MGT user clocks.

### 3. Test benches: simulation and example design

As opposed to the GBT-FPGA project, no example designs are included into the main LpGBT-FPGA repository. However, two test benches are available as independent projects: one as a simulation testbench (using QuestaSim), the other one as a hardware implementation (for KCU105). They shall not be re-used as they are in complex designs, but rather considered as examples of implementation or as test platforms to check the functionality and measure the performance of the LpGBT-FPGA core.

The architecture of the two test benches, shown in Figure 3, is the same. Because the front-end chip is not yet available, a part of the LpGBT ASIC's logic dedicated to SERDES functions is used to emulate the front-end encoding/decoding functions and is implemented as an "LpGBT Emulator" (in white). The LpGBT-FPGA core (in blue) is complemented with an MGT (in orange) and surrounded with pattern generators and checkers (in grey). Error injectors (in red) are also provided to simulate data corruption similar to the expected failures caused by SEUs in high-energy physics experiments (burst). The only difference between the hardware implementation

and the simulation is the MGT module: the simulation is based on a simple emulation of a transceiver when the KCU105 design uses the Xilinx GTH IP. The block diagram below shows the test platform environment.

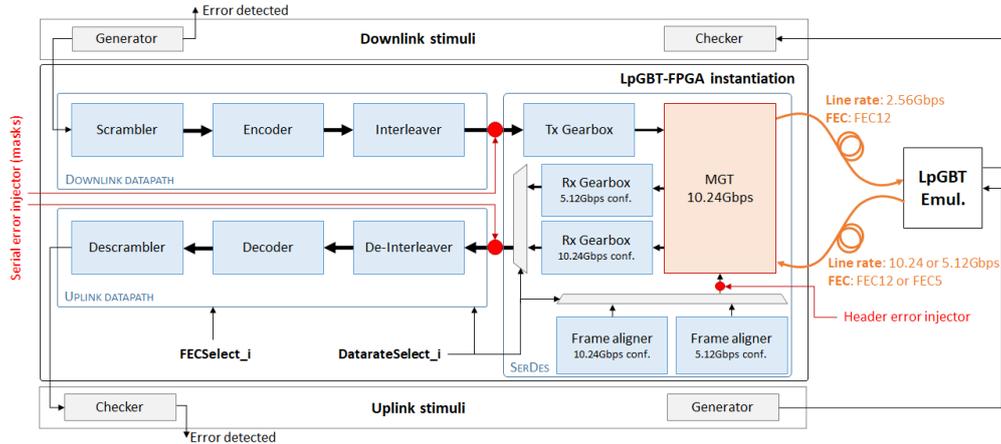


Figure 3: LpGBT-FPGA Test benches architecture

In order to propose test benches generic enough to test all of the uplink configurations using the same logic, the LpGBT-FPGA features a ‘dynamic mode’ instantiating all the FEC and Data rate modes. This avoids compiling the design for each case and allows dynamic reconfiguration of the FEC/rate for testing purpose. However, this mode is not recommended for final design as it duplicates the logic as shown in the block diagram below (Figure 4). When the IP is set in dynamic mode, the MGT must indeed be configured for 10.24Gbps in both directions, the rate reduction being handled, if necessary, by oversampling gearboxes. Some logic duplication is also necessary in the data path in order to allow selecting dynamically the decoding scheme (FEC5 or FEC12). On the contrary, when the IP is implemented to run at a specific speed (‘static mode’), only one Rx gearbox and one frame aligner are required. In this case, the MGT can also be specifically targeted and optimized to work at the selected upstream data rate. The table 2 below shows the resource utilization for the configuration selected for the KCU105 test bench.

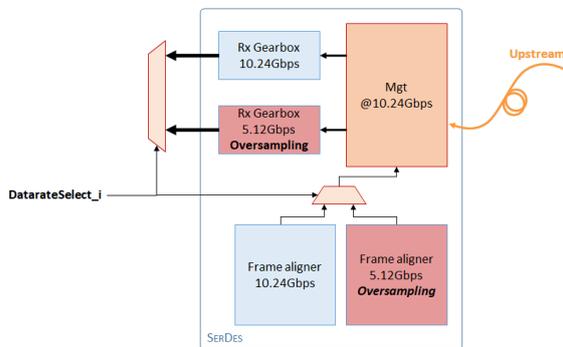


Figure 4: SerDes implementation in dynamic mode

		Resource usage	
		LUT	KCU105
Downlink	Data path	100	0.04%
	SerDes *	150	0.06%
Uplink	Data path	2348	0.97%
	SerDes *	551	0.23%
MGT	Transceiver	186	0.07%

\* Includes gearboxes and frame aligners

Table 2: KCU105 resource usage

#### 4. Status and future plans

The first version of the LpGBT-FPGA was released in July 2018 [2]. It came with a simulation test bench, used in QuestaSim. The first hardware test bench was developed and has just been released.

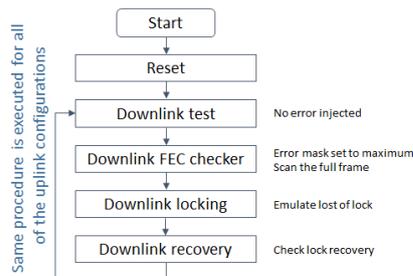


Figure 5: LpGBT-FPGA behavioural test

The continuous integration tools, supported in GitLAB at CERN, provide a way to automatically run the simulation every time a new version of the IP is being pushed. Therefore, a script was designed to automatically check the core functionality, and especially the correction capability of the modules. The algorithm presented on the Figure 5 describes the procedure systematically used to check the LpGBT-FPGA core behavior.

Once the core had been successfully validated using this model, a new test bench targeting the KCU105 development kit from Xilinx was designed to check the timing aspect and carry out some tests with real transceivers and optical fibers. A first bunch of tests, consisting of data integrity checking and latency monitoring, was carried out. Further series of measurements are foreseen to be performed upon LpGBT prototypes delivery.

After having ensured a successful compilation and timing-closure of the design targeting the Xilinx Kintex Ultrascale FPGAs, additional modules were added for the LpGBT-FPGA control and monitoring. They mainly consist of ILAs, VIOs and a JTAG-To-Axi controller in order to perform automatic resets, to check the locking state and to measure the downlink latency. These control and monitoring modules were used to perform a first latency measurement with the LpGBT emulator (a simplified synthesizable version of the LpGBT serdes). This result will certainly change with the final component but the first result is encouraging with a downlink latency of 155ns and a stability between Tx and Rx clocks, using the HPTD module [3], of 12ps.

The upstream qualification will consist in measuring the coding gain and the impact of the dynamic mode. The downstream characterization will focus on latency and coding gain. These tests are planned to be done using the first validated prototypes (LpGBT and VTRx+). The block diagram (Figure 6) illustrates the test setup.

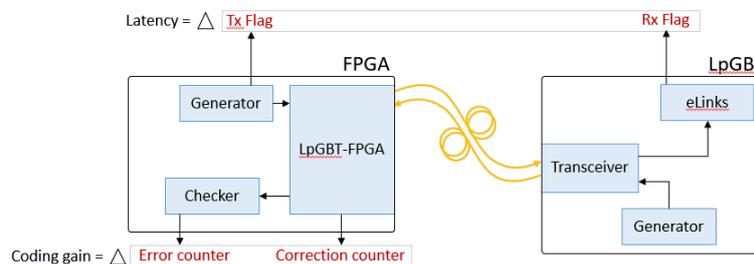


Figure 6: Test setup planned to be used for the LpGBT-FPGA qualification

A further step will consist in the development of a slow control module to handle the Internal control field and the integration of the GBT-SC IP to communicate with the GBT-SCA. Last but not least, the complete setup will be essential for the LpGBT ASIC testing.

## References

- [1] LpGBT ASIC: <https://espace.cern.ch/GBT-Project/LpGBT>
- [2] Project Gitlab: <https://gitlab.cern.ch/gbt-fpga>
- [3] HPTD IG page: <https://espace.cern.ch/HighPrecisionTiming>