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New LpGBT-FPGA IP: Simulation model and first implementation

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High speed links are commonly used in High Energy Physics experiments for data acquisition, trigger and timing distribution. For this reason, a radiation-hard link is being developed in order to match the increasing bandwidth demand of the backend electronics and computing systems. In this framework, the LpGBT -which is the evolution of the GBTx SERDES- is being designed and is foreseen to be installed in CMS and ATLAS for Phase-2 upgrades. The LpGBT-FPGA IP core is proposed to offer a backend counterpart of the LpGBT. This paper presents the status of its development, the IP architecture and the future steps.

Summary

The LpGBT ASIC (Low Power GigaBit Transceiver) is a new 65nm-CMOS radiation tolerant serializer/deserializer device that can be used on the front-end electronics of the HL-LHC detectors. This component is foreseen to be used by CMS and ATLAS for their system upgrades and offers a set of encoding and decoding schemes specifically tailored to meet their needs in terms of radiation-hardness and data bandwidth.
The LpGBT-FPGA project started in 2018 as a natural evolution of the existing GBT-FPGA to provide a back-end counterpart to the future LpGBT ASIC. The new FPGA IP implements the encoding/decoding schemes supported by the front-end ASIC, meaning that it can be configured using 4 different combinations for the upstream link (from Front-end to Back-end): two decoding schemes (FEC5 or FEC12) based on Reed-Solomon techniques to configure the encoding robustness and two line rates (10.24 or 5.12Gbps) depending on the required bandwidth. Additionally, the LpGBT-FPGA core features an asymmetric architecture to match the LpGBT ASIC specificities: the transmitter part of the IP, as opposed to the configurable receiver part, proposes a single encoding scheme (FEC12) and a lower line rate of 2.56Gbps. Such an asymmetry prevents the IP to be used in loopback mode for self-testing. A behavioural model of the LpGBT will therefore be used for simulation and –to fill the gap until the LpGBT ASIC distribution- a hardware platform and a firmware IP emulating the ASIC will be required for hardware testing.
This paper will present the LpGBT-FPGA core in detail, focussing on its architecture, its interfaces and its available features: dynamic and static configuration, encoding/decoding, scrambling/descrambling, error counters, etc. It will also discuss the infrastructure proposed around this core, and in particular the ASIC model and its hardware and firmware emulator. It will finally introduce the first characterization of the IP with the first latency measurement using the emulator system and discuss dynamic versus static data rate configuration performance in term of coding gain.

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