The CMS detector is undergoing a system-wide upgrade, and specifically the complete redesign of the end-cap sub-detectors for the High Luminosity LHC (HL-LHC).

To reach the aimed 30 ps RMS timing resolution, a precision clock distribution system providing a readout clock with a sub 15 ps RMS jitter is mandatory.

A detailed study on the current technologies as well as an extensive discussion of the R&D dedicated to the low-jitter clock distribution are presented.

### CMS detector

The CMS detector is made of concentric layers of different sub-detectors arranged around the collision point. It is designed to precisely measure the properties of the particles produced after each collision in a harsh radiation environment.

### CMS electronics

- **Detector data & control**
  - 4x12 100 Gbps L1 trigger data link
  - Trigger Control and Distribution System (TDCs)

- **Detector & End-Front-End (FE)**
  - ATCA crate
  - OTH readout links (2) on ATCA board

- **Phase II electronics architecture** will be based on the PICMG ATCA standard
  - 40 MHz synchronous readout, data & trigger paths are separated
  - Central DAC and TTC hub (DTH), 1 or 2 per ATCA crate
  - 175 MHz trigger rate using 50 000 high-speed front-end optical links for an average 7.5 ps per event
  - Radiation hard and magnetic field tolerant on-detector Front-End electronics

### CMS Phase II upgrade at HL-LHC

Planned for commissioning by 2023, Phase II upgrades include:

- The full replacement of tracker and end-cap calorimeters (electromagnetic and hadronic)
- New end-cap calorimeter design based on a high granularity architecture using high precision time detectors
- New NIF time detector between tracker and calorimeters foreseen to further enhance timing measurements to cope with high pile-up (up to 200)
- Complete redesign of the Electromagnetic Barrel Calorimeter electronics with enhanced timing precision

The upgrade program aims for a timing precision of 30 ps for particles with energy over 50 GeV.

- To reach this goal, a high precision clock distribution (~15 ps) is necessary.

### Studies of the baseline encoded clock distribution

- Measuring the clock jitter after each step of the current clock distribution scheme as shown above
- The clock path uses the following steps:
  - BE DAC board encodes the clock within the high speed data stream of the control link
  - 5 Gbps clock and command controls are sent to on-detector FE electronics via up to 100 M optical cables using custom-GMIB protocol
  - FE electronics recovers the clock using GBS chip’s Clock and Data Recovery (CDR) feature
  - GBS chip forwards the clock to VFE electronics through custom optical connection

### MicroTCA clock distribution studies

- **Measurement point**
  - Output of the ATCA backboard
  - Bit error rate (BER) results

<table>
<thead>
<tr>
<th>Measurement point</th>
<th>Clock frequency</th>
<th>Random jitter</th>
<th>Deterministic jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference clock</td>
<td>407 MHz</td>
<td>&gt; 5 ps</td>
<td>&lt; 1 ps</td>
</tr>
<tr>
<td>Optical clock</td>
<td>1176 MHz</td>
<td>30.6 ps</td>
<td>4.8 ps</td>
</tr>
<tr>
<td>Output of ATCA</td>
<td>407 MHz</td>
<td>30.6 ps</td>
<td>26.5 ps</td>
</tr>
</tbody>
</table>

### Front-end clock distribution studies

- **Measurement description**
  - Single BE - Single FE - Two link clock
  - Single BE - Two FE - Two link clock
  - Two BE - Two FE - Two link clock

<table>
<thead>
<tr>
<th>Measurement description</th>
<th>Random jitter</th>
<th>Deterministic jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single BE - Single FE</td>
<td>7.6 ps</td>
<td>3.4 ps</td>
</tr>
<tr>
<td>Single BE - Two FE</td>
<td>8.7 ps</td>
<td>22.1 ps</td>
</tr>
<tr>
<td>Two BE - Two FE</td>
<td>13.7 ps</td>
<td>12.7 ps</td>
</tr>
</tbody>
</table>

### PLL loop bandwidth effects on clock jitter

Programmable loop bandwidth of the jitter clearing PLL can be very efficient in reducing clock jitter but needs tuning to optimize it.

Tests demonstrated that a too narrow loop bandwidth results in folding up the phase noise in lower frequency offsets, increasing the total jitter of the clock.

### Full chain clock results using current electronics

- **Measurement description**
  - Two 8x144 PLLs - Two BE & FE - Two clock paths

<table>
<thead>
<tr>
<th>Measurement description</th>
<th>Random jitter</th>
<th>Deterministic jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two 8x144 PLLs - Two BE &amp; FE - Two clock paths</td>
<td>11.2 ps</td>
<td>38.7 ps</td>
</tr>
</tbody>
</table>

Clock jitter measurements give encouraging results indicating that the specifications for Phase II upgrades are within reach but still require extensive R&D to deal with deterministic jitter.

### Summary

- CMS Phase II upgrade aims for a precision of 30 ps for particles with energy over 50 GeV (including clock, detector and electronics contributions)
- Studies on Precision Clock Distribution solutions are ongoing at IRFU, CEA, Saclay, to achieve the required 15 ps RMS clock jitter precision (in collaboration with CERN)
- Encoded clock distribution option tested in laboratory conditions with current technology holds the promises of attaining the specs. Scalability is still to be confirmed
- Online and offline monitoring and alternative pure clock distribution solutions under investigation
- The CMS Phase II upgrade R&D is still ongoing and final electronics are not yet available.
- Results using all foreseen Phase II components expected by TWEPP 2019

### Next steps

- Development of monitoring solutions to cope with wander (slow phase drift)
- Characterization of temperature effect on phase drift in optical cables and electronics
- Update of the test bench while Phase II technologies and components become available
  - ATCA FE boards: DAC & TDCs Hub board (DTH), BE DAC boards (eg. Serenity and BCP)
  - Detector FE core electronics: lpsGRT chip and the lpsGRT-FPGA IP
  - CMS Phase II FE read-out electronics: e.g. HGROC chip for end-cap sub-detector (HgCal)
- Investigating a dedicated clock distribution solution with separated clock and data paths

### Clock distribution studies for O (10 ps) precision timing with high speed electronics in very large distributed O (100 m) acquisition system with several million channels working in high radiation environment

TWEPP 2018: Topical Workshop on Electronics for Particle Physics 17-21 September 2018, KU Leuven