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Development and testing of a Trigger Processor Card based on a Kintex Ultrascale FPGA

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A trigger processor demonstrator card has been designed for the CMS Barrel Muon Trigger (BMT) upgrade at HL-LHC. A two-layer system design is foreseen for BMT. Layer-1 hosts the trigger primitive algorithms and preliminary tracking algorithms. Layer-2 hosts the main track finding algorithm, the correlation between the tracks from the muon system and the track-trigger for best possible estimate of the muon momentum. The processor card is a demonstrator for Layer-1 and is instrumented with a Kintex UltraScale FPGA and optical links at 16 Gbps. The Hardware and Firmware design as well as information of the performance is presented here.

Summary

The upgraded High Luminosity LHC, after the third Long Shutdown (LS3), will provide an instantaneous luminosity of 7.5 10^{34} cm^{-2} s^{-1} (levelled), at the price of a dramatic increase of the number of pileup interactions. It is generally expected that the number of pileup interactions could reach 200 per bunch crossing. The upgraded detector will be read-out at an unprecedented data rate of up to 50 Tb/s and an event rate of 750 kHz.

Within the scope of Phase 2 R&D, a new Level-1 Trigger processor card was designed, to provide a hardware environment for developing and evaluating new Level-1 trigger muon designs and technologies.

The board is powered by a Kintex UltraScale FPGA, that provides the best price/performance/watt at 20nm technology and includes the highest signal processing bandwidth in a mid-range device. The Kintex UltraScale FPGA provides 20 next-generation GTY transceivers that reach speeds up to 16.3 Gbps.

The board comes with state-of-the-art fibre optics technologies, from Samtec, using micro footprint optical interconnects that enables chip-to-chip, board-to-board, and system-to-system connectivity. The high performance interconnect system uses active optical engines, that provide 12 full-duplex channels, at data rates up to 28 Gbps, more than enough to accommodate the 16 Gbps speed of the FPGA transceivers. Furthermore, 4 FPGA transceivers are routed to a QSFP28 connector, allowing data rates of up to 28 Gbit/s per channel over 4 channels. In total the board's 16x16 Gbps links add up to a total optical bandwidth of approximately 256 Gbps in each direction, making it a high-performance all-optical, data-stream processor.

A Xilinx ZYNQ System-on-Chip (SoC) device will be used as the control interface for the Kintex UltraScale FPGA. The system controller sets up or queries on-board resources, such as the power controllers and a programmable clock. A DDR4 component memory was also included to allow the ZYNQ device to run a lightweight, embedded Linux OS.

For testing purposes, a new firmware was developed, implementing synchronous and asynchronous 16Gbps GTH links with error detection. The links use the 64b/66b encoding scheme with an overhead of 2 coding bits per 64 bits, that is considerably more efficient than the previously-used 8b/10b encoding scheme. In addition, a simple infrastructure with input/output buffers and IPBus support, was developed to accommodate the testing of new algorithms. The hardware and firmware design of the processor card is presented here.

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