Ultraflex: An ATCA prototype board for the CMS Phase 2 Tracker Upgrade

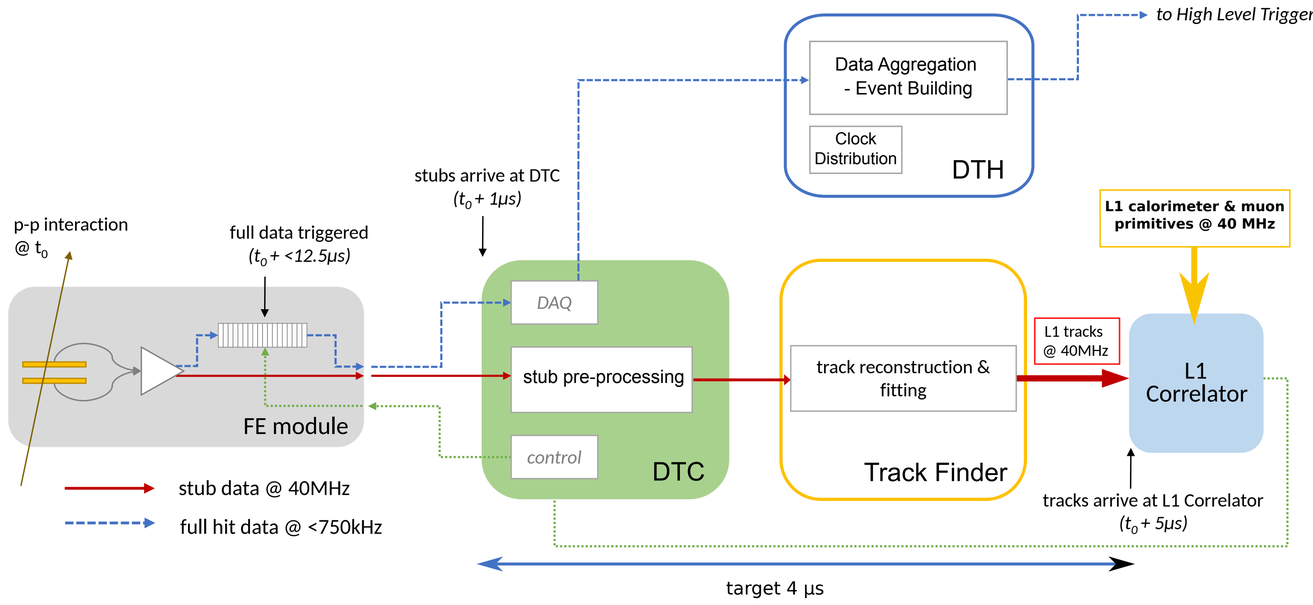
Luis Ardila-Perez, Oliver Sander, Thomas Schuh, Matthias Balzer, Marc Weber, Luigi Calligaris, André Cascadan, Vitor Finotti, Sthefany de Souza, Alison França Queiroz da Costa, Ailton Akira Shinoda, Lucas Arruda Ramalho
luis.ardila@kit.edu

Track Finder Architecture

Two stages of data processing
- ▸ **DAQ, Trigger and Control (DTC)**
- ▸ **Track Finding Processor (TFP)**

Two central data concentrators per crate
- ▸ **DAQ and TTC Hub (DTH)**

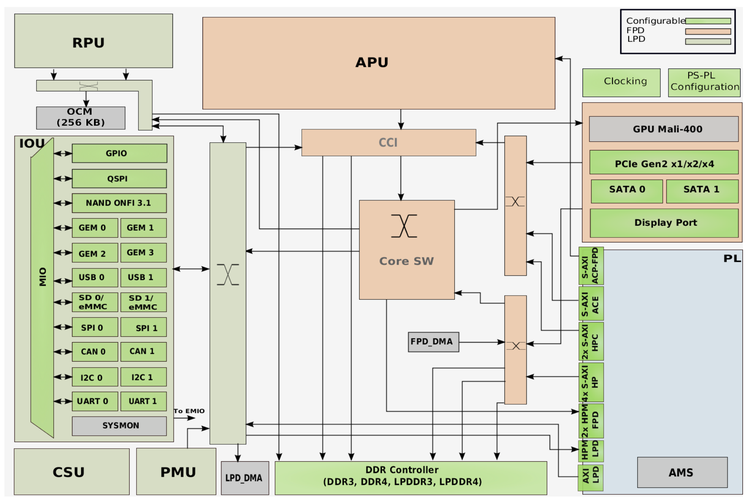
- ▸ **All-FPGA** processing system
- ▸ **ATCA** form factor with dual-star backplane



Tracker Backend R&D

Several technologies are being evaluated for the tracker upgrade with the aim of reaching a common definition about:
- ▸ **Slow Control**
- ▸ **IPMC**
- ▸ **System Monitoring**
- ▸ **On-Board Processor**
- ▸ **TCDS Distribution**
- ▸ **ATCA requirements**
- ▸ **JTAG & Backdoors**

Zynq Ultrascale+ MPSoC Features



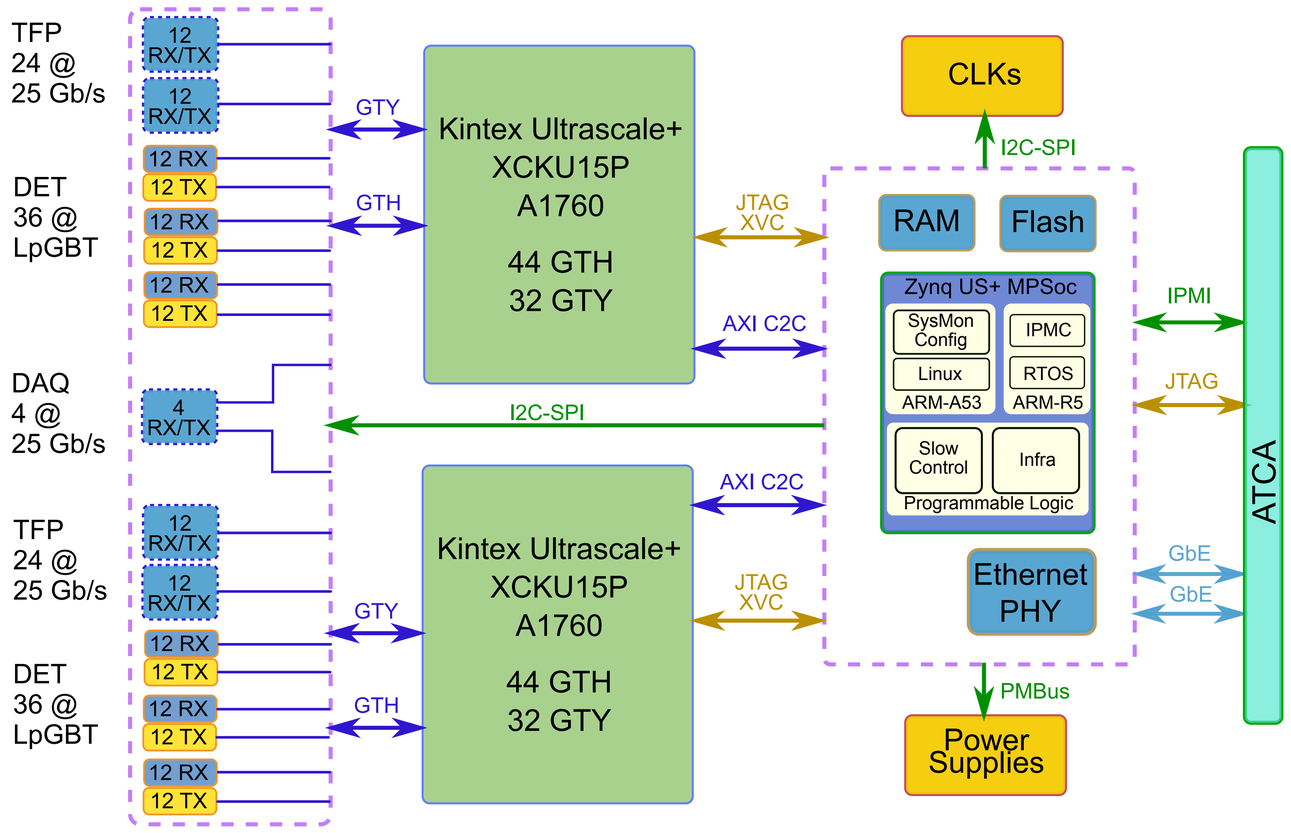
- ▸ **Independent power domains** where each sub-system can be powered up, powered down, restarted or suspended without affecting the other sub-systems
- ▸ Real time capable processor for time critical applications
- ▸ Powerful quad core ARM-A53 processor capable of running yocto based linux
- ▸ Ability to configure the processing units in Symmetric and Asymmetric Multiprocessing (SMP, AMP) modes as well as inter-core communication via OpenAMP
- ▸ FPGA logic and high-speed transceivers tightly coupled to processing system

Conclusions

- ▸ Trend to integrate more infrastructure slow control functionality on ATCA boards
- ▸ We propose to integrate IPMC, GPP based slow control functionality and FPGA in one single heterogeneous MPSoC (Zynq Ultrascale+)
- ▸ Utilizing a single device propose integration benefits to back-end administrators

UltraFlex ATCA Board

- ▸ Centralized slow control and board management solution based on Zynq Ultrascale+ System-on-Chip
- ▸ Two main FPGAs Xilinx KU15P with all high-speed links connected to expandable mezzanine
- ▸ Application specific high-speed mezzanine
- ▸ ATCA form factor

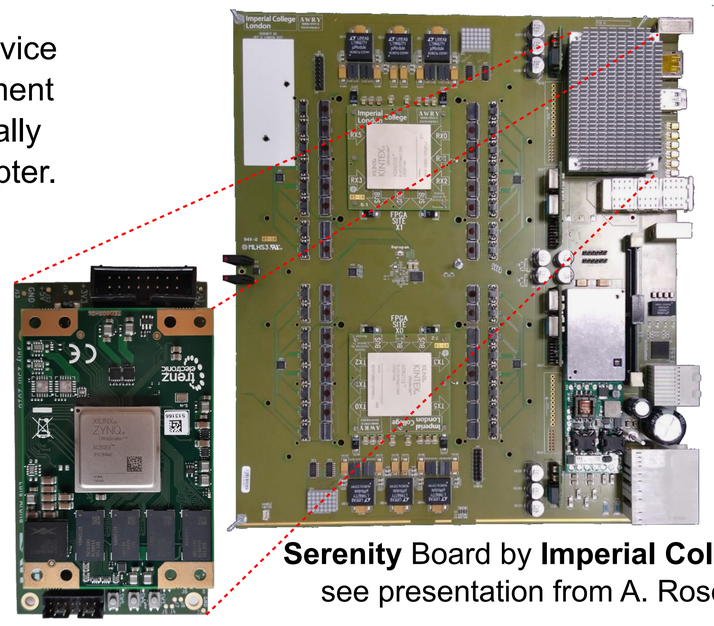


Proof of concept with Serenity-Zynq Adapter

Evaluate the concept of a unique device for slow control and board management using Serenity board and commercially available Zynq US+ module via adapter.

Slow control to main FPGAs
- ▸ **PS_PCIe** to Site **X0**
- ▸ **PL_C2C** to Site **X1**

- ▸ **IPMI** to backplane
- ▸ **PMBus** to config Power supplies
- ▸ **I2C** to Clock chips
- ▸ **Ethernet**
- ▸ USB 2.0



Serenity Board by **Imperial College**
see presentation from A. Rose.

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