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Ultraflex: An ATCA Prototype Board for the CMS Phase 2 Tracker Upgrade

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Currently, various hardware concepts and technologies are being evaluated for the CMS Phase 2 Tracker off-detector processing system. The back-end electronics system comprises the Data Trigger and Control (DTC) system, the Track Finding Processors (TFP) and the DAQ \& TTC Hub (DTH). We designed UltraFlex as an ATCA based technology demonstrator with two main purposes: to implement a flexible approach to evaluate different optical high-speed transceivers and to provide a novel centralized slow control and board management solution based on Zynq Ultrascale+ (US+) System-on-Chip (SoC).

Summary

Currently, various hardware concepts and technologies are being evaluated for the CMS Phase 2 Tracker off-detector processing system. An essential part of the back-end electronics system are the Data Trigger and Control (DTC) boards, which receive tracking data, as well as raw data from the outer tracker modules. Tracking data, also called stubs, are forwarded to the Track Finding Processors (TFPs) for track reconstruction for the L1 trigger. In the case of triggered events, raw data are received from the outer tracker, aggregated and forwarded to the DAQ \& TTC Hub (DTH) boards. The system requires a large number of high-speed optical links with up to 25 Gbps per lane between boards. Therefore we developed UltraFlex, an ATCA based demonstrator card, which is meant to evaluate different optical transceiver technologies, in addition to a highly integrated board management and slow control concept.

The central processing elements on the UltraFlex ATCA board are two Xilinx XCKU15P devices. All their high-speed links are routed to a daughtercard using the new Samtec Z-Ray interposer. This daughtercard carries all optical transceivers such as Samtec Firefly, Finisar BOA, PAM4, etc. By doing so, optical transceivers can be easily exchanged using another daughtercard. While daughtercards have a limited complexity, their development is simple compared to an entire ATCA board redesign. The daughtercard also allows designers to daisy chain the two FPGAs if required by another application.

Furthermore, UltraFlex explores the idea of using a highly integrated solution for board management and slow control. It carries a Xilinx Zynq US+ heterogeneous System-on-Chip (SoC) which provides FPGA logic, high-performance ARM-A53 multi-core processors and two ARM-R5 real-time capable processors. The ARM-R5 cores are used to implement time-critical and deterministic tasks using freeRTOS. They carry out the IPMI/IPMC functionality and communicates via backplane with the shelf manager at power-up. The ARM-R5 are also connected to the power supply (via PMBus), to voltage and current monitors, to clock generators and jitter cleaners (via I2C, SPI) providing the required configuration at start-up. Once full power is enabled from the crate, a Yocto based Linux starts on the powerful ARM-A53 cores. For slow control the SoC is the central entry point to the two Kintex US+ FPGAs, it provides Ethernet interfaces for TCP/IP protocols, IPBus and the like. The communication between the Zynq US+ SoC and the Kintex US+ FPGAs uses the AXI chip-to-chip protocol via LVDS lines. With that none of the high-speed transceivers is required for slow control. Finally, The AXI memory-mapped protocol is used inside the main Kintex US+ FPGAs thereby requiring a low amount of resources.

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