# Front-end hybrids for the strip-strip modules of the CMS Outer Tracker Upgrade

T. Gadek[1], G. Blanchot[1], R. Gajanec[2], A. Honma[1], M. Kovacs[1]

[1]CERN, Route de Meyrin, CH-1211 Geneva 23, Switzerland, [2]Slovak University of Technology, FEEIT, Ilkovicova 3, 812 19 Bratislava, Slovakia

Contact info:
*tomasz.gadek@cern.ch*
*georges.blanchot@cern.ch*
*mark.istvan.kovacs@cern.ch*

## Abstract

*The CMS Outer Tracker planned for the HL-LHC Upgrade contains strip-strip and pixel-strip silicon modules. Each of them includes two high-density front-end hybrid circuits, equipped with flip-chip ASICs, passives, connectors and mechanical structures. Several strip-strip hybrid prototypes have been produced using the CBC2 front-end ASIC. Feedback from these developments helped improving the hybrid's testability and the production yield. The availability of the concentrator ASIC's footprint and of the new CBC3 front-end ASIC enables the design of all strip-strip hybrid variants. In this work the development milestones and the final designs are presented together with chosen solutions.*

## Strip-strip modules for CMS Outer Tracker Upgrade

The CMS Outer Tracker planned for the HL-LHC will consist of 7680 strip-strip (2S) modules. Each module is build with two parallel sensors of 2032 strip lines each, two front-end read-out hybrids and a service hybrid. The role of the service hybrid is to provide the optical data connectivity outside of the module, to bring powering for the front-end hybrids and the biasing for the sensors. The front-end hybrids host 8 front-end ASICs named CBC, which make the necessary hit correlation and produce data outputs in a digital format via 6 SLVDS ports each. These 48 data streams are aggregated in the concentrator ASIC (CIC) and send to the service hybrid through a fine pitch connector. The concept of the mechanical structure of the 2S module and the principle of the hit correlation, also know as the "stub" detection, are shown in the figures below.

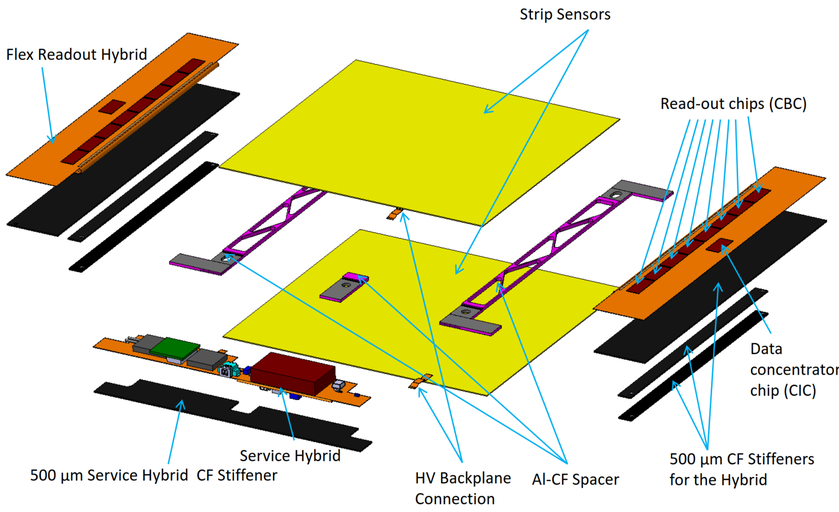


Fig.2: An exploded view of a conceptual 3D design of the Strip-Strip Module.

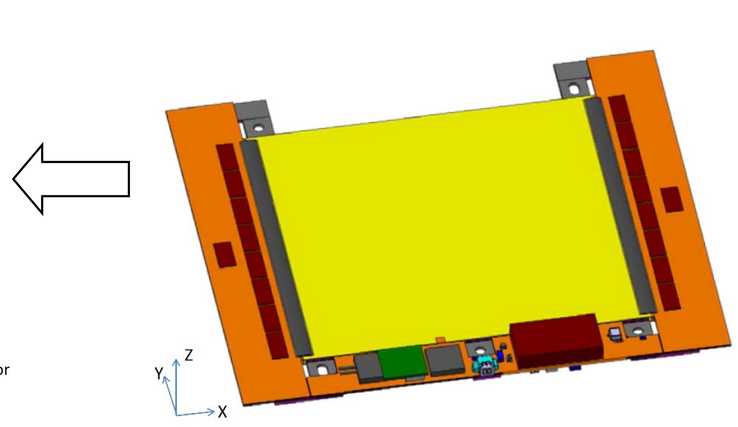


Fig.1: A conceptual 3D design of an assembled Strip-Strip Module.

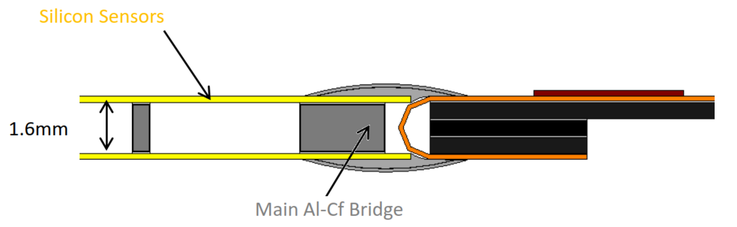


Fig.3: A cross section view showing wire bond interconnections of both sensors to a folded front-end hybrid.

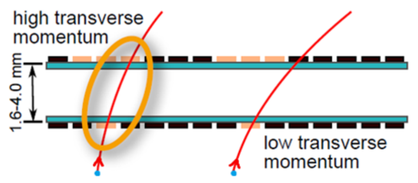


Fig.4: A cross section view explaining the idea of double-sensor use for high-momentum particles' discrimination.

## Prototype front-end hybrids with 2 CBC3 ASICs

In 2017 a third generation of the CBC front-end ASIC has become available. This version of the CBC implements the full functionality expected from the 2S front-end ASIC: data rates of 320 Mbps, hit correlation logic with adjustable window search of "stub" (high transverse momentum particle crossing) events and a chip to chip communication for the detection of particles crossing edge channels of two ASICs. A new hybrid circuit was designed to test the chip's functionality and its new features.

The flex circuit hosts just 2 CBC3 ASICs and implements the target 2S hybrids' 4-layer stack-up with total thickness of approximately 150 µm. The build-up of the hybrid was simplified by using two FR4 stiffeners instead of 3 carbon fibre pieces. The hybrid was the first of its family running with a clock at 320 MHz. A few test features were hosted on board: an access to the analogue multiplexers of the CBCs, probing points for 40 MHz clock, temperature monitoring and a high voltage filter for the sensor biasing.

25 hybrids were produced and successfully qualified. Two minor undesired features were discovered in the ASIC and will be corrected in its 3.1 version. A few hybrids were equipped with silicon sensors and tested in test beam facility at Fermilab. The test campaign demonstrated that the stub finding efficiency is very high (>99%) and that the transverse momentum cut-off is as expected for the sensor strip pitch and spacing.

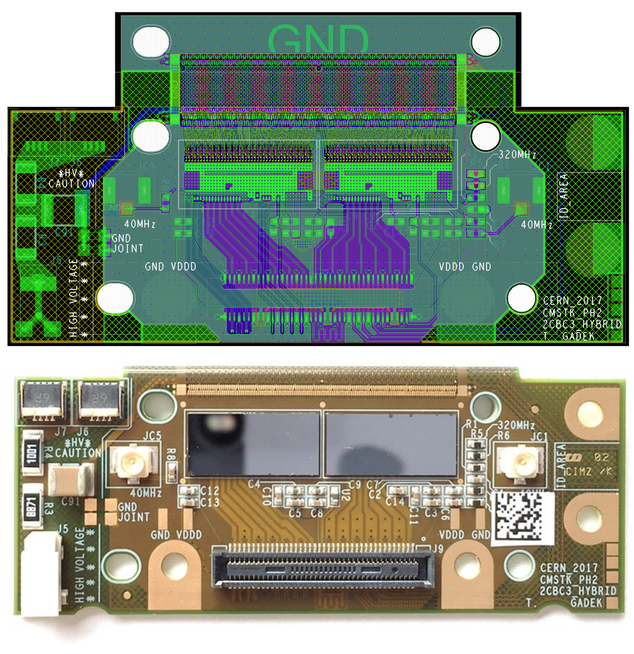


Fig.5: Layout of a 2CBC3 flex (top) and a photo of a folded and assembled 2CBC3 hybrid (bottom).

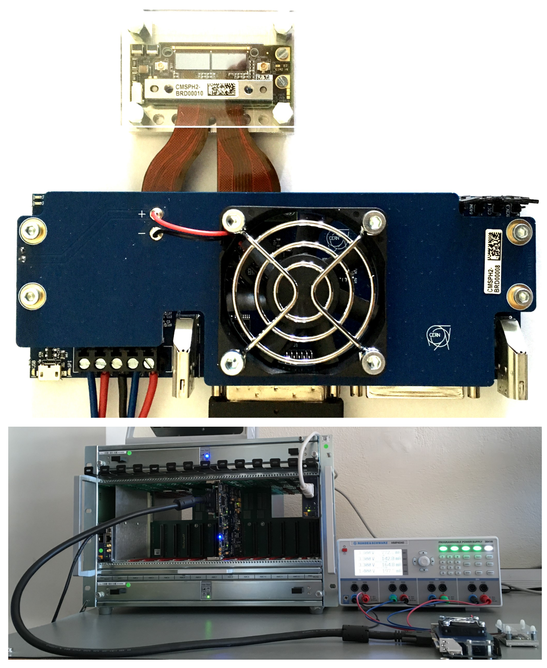

Fig.6: Photo of a 2CBC3 connected to an interface board (top) and a photo of an uTCA FPGA based test system with the interface board (bottom).

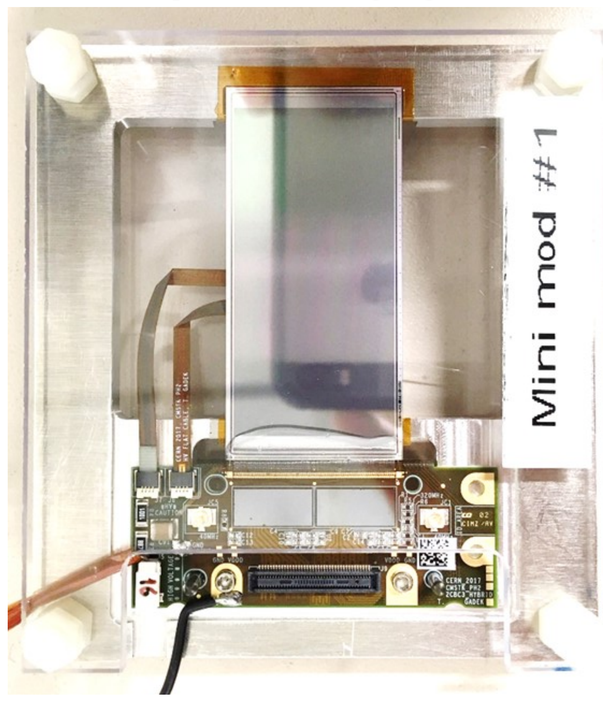


Fig.7: Photo of a mini module built with a 2CBC3 hybrid and two silicon sensors with 254 strips each (5 cm by 90 µm).

## Prototype front-end hybrid design with 8 CBC3 / CBC3.1 ASICs

After a successful production of 2 CBC3 hybrid, a larger object is needed, which enables production of a full size prototype 2S module. This new 8-ASIC circuit will host both CBC3 and CBC3.1 chips. Assembled hybrids should arrive in Q3/Q4 2018. The flex still misses the concentrator ASIC, which bumped version should be available to the community in 2019. In the meantime the functionality of CIC will be substituted by a back-end FPGA interconnected via two 100-pin fine pitch connectors. Additionally a mezzanine board hosting a wire-bonded version of CIC is being designed. The board is meant to be plugged directly onto the hybrid's connectors.

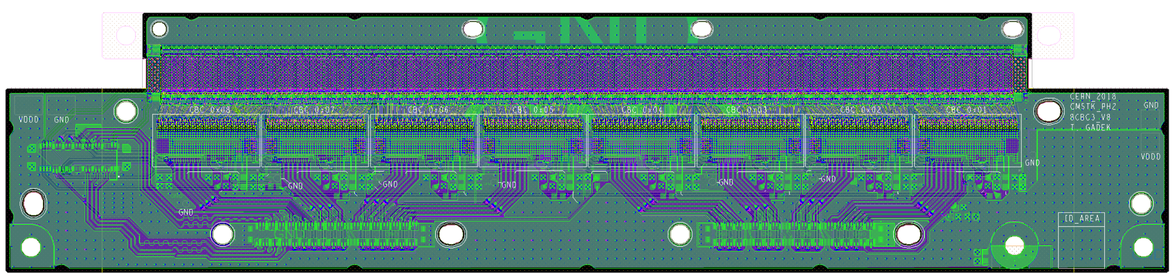


Fig.8: Layout of an 8CBC3 flex.

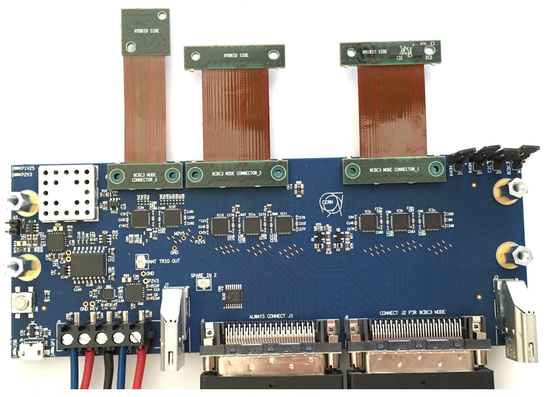

Fig.9: Photo of an interface card with flex interconnections for 8CBC3.

## Complete 2S front-end hybrid design

A bump map and a preliminary pin assignment of the CIC became available in Q3 2018. This enabled a complete 2S front-end hybrid design. The hybrid fulfills all the dimensional and mechanical requirements up to date. It is compatible with the latest Service Hybrid requirements and connector's pin assignment. It was fully routed following the manufacturing constraints and implementing all necessary testing features. The design was studied and improved in terms of voltage drop budget across the power and return plane, which are now well balanced. Further simulations are planned after the 8CBC3 characterization.

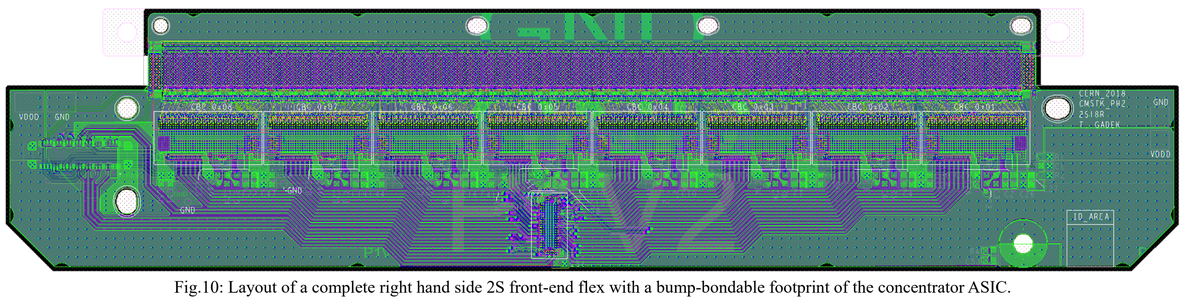


Fig.10: Layout of a complete right hand side 2S front-end flex with a bump-bondable footprint of the concentrator ASIC.

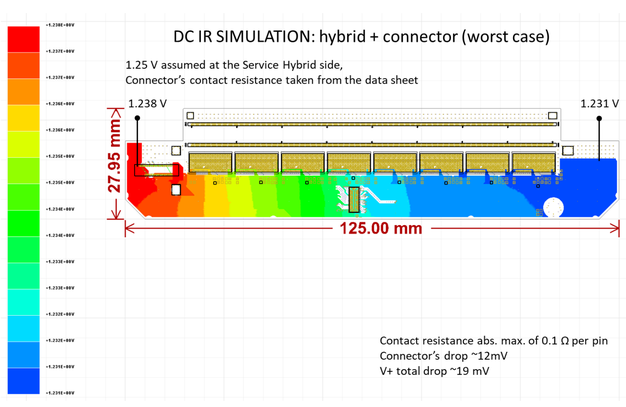


Fig.11: Picture of a voltage drop simulation of the 2S front-end hybrid flex design.

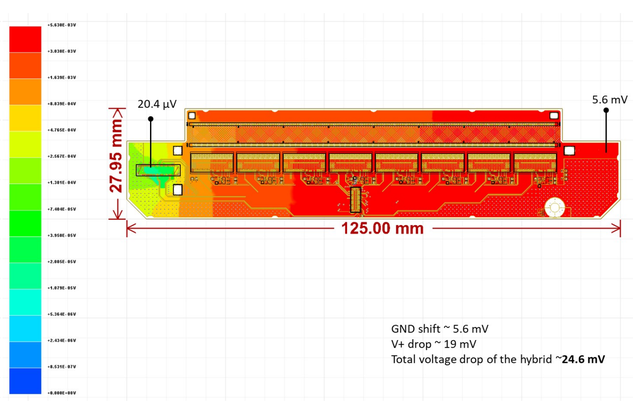


Fig.12: Picture of a ground shift simulation of the 2S front-end hybrid flex design.

## Future development

The development of the 2S type hybrids is approaching the production phase. The last planned prototype, which is the 8CBC3 / 8CBC3.1 hybrid is in production and due to Q3/Q4 2018. The experience gained from this production batch will guide changes, if necessary, in the final 2S front-end hybrid design. 2S hybrids' development is well in line with planned CIC submission for a bumped version with full functionality expected from that ASIC. Any modifications in the ASICs footprints will be incorporated in order to start the pre-production phase in 2019.

## Conclusion

The CMS Outer Tracker planned for the HL-LHC Upgrade contains 7680 strip-strip silicon modules. Each of them includes two high-density front-end hybrid circuits, equipped with flip-chip ASICs, passives, connectors and mechanical structures. Two strip-strip hybrid prototypes have been designed using the CBC3 front-end ASIC. Feedback from these developments helps improving the front-end ASIC itself and guides the designs of final 2S hybrids. The availability of the concentrator ASIC's footprint and of the new CBC3.1 front-end ASIC enabled the first complete design of the 2S front-end hybrid. The design in the current shape is ready for the pre-production phase of the project.