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Front-end hybrids for the strip-strip modules of the CMS Outer Tracker Upgrade

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The CMS Outer Tracker planned for the HL-LHC Upgrade contains strip-strip and pixel-strip silicon modules. Each of them includes two high-density front-end hybrid circuits, equipped with flip-chip ASICs, passives, connectors and mechanical structures. Several strip-strip hybrid prototypes have been produced using the CBC2 front-end ASIC. Feedback from these developments helped improving the hybrid's testability and the production yield. The availability of the concentrator ASIC's footprint and of the new CBC3 front-end ASIC enables the design of all strip-strip hybrid variants. In this work the development milestones and the final designs are presented together with chosen solutions.

Summary

The operation of HL-LHC imposes demanding requirements on the particle detectors. The luminosity will be raised by a factor of 10 beyond the original LHC design value, which results in higher radiation and data rate. A complete replacement of the CMS Outer Tracker is foreseen to adapt to this new environment. Its design is optimized to provide the most useful information about interesting trajectories of collision's products, reducing the necessary data flow. To achieve these goals several features are implemented at the level of front-end modules, such as lower mass, Level 1 track triggering functionality, data compression and a higher density of sensing channels.

The functional building blocks of the future tracker's structure are based on two types of double-sensor modules: pixel-strip (PS) and strip-strip (2S). The 2S modules will be produced in two versions that vary in the distance between their sensor planes. Each module contains two high-density front-end hybrid circuits. In the 2S module, hybrids host eight binary readout flip-chip ASICs (CBC) and a data concentrator ASIC (CIC), which aggregates and serializes digital information received from CBCs. Additionally, each hybrid is equipped with passive components and mechanical reinforcement structures, which also serve as a cooling interface. In total four different 2S front-end hybrid geometries are foreseen in the project. It is planned to use 15,360 hybrids of this type inside of the CMS tracking volume.

Following a preliminary development of a 2CBC3 hybrid variant used for qualifying the new front-end ASIC and its associated testing features, the four final 2S hybrid variants have been designed in 2018. They match the geometry driven by recent modules'models and are a result of a long development path of prototype hybrids. The 2CBC3 carrier received and tested by the end of 2017 provided crucial information on the lateral communication feature of the front-end chip. It also served as a validation platform for the implemented routing methodology and test features thus giving a green light for a larger 8CBC3 object (still without CIC chip). This new full-size hybrid shall be available for qualification in Q3 of 2018 and will be used to evaluate the final CBC3.1 front-end ASIC that is footprint and pinout compatible with the CBC3. In the meantime, a design of the data concentrator has matured enough to derive its first footprint and pin assignments. Consequently, a full routing exercise of all the 2S front-end hybrid variants became possible.

This work will report on the 2CBC3 design and results, followed by its expansion towards the 8CBC3 focusing on the final hybrid geometry and features. Ultimately, the integration of the CIC into final 2S hybrids, all variants included, will be discussed.

Primary author: GADEK, Tomasz (CERN)

Co-authors: HONMA, Alan (CERN); BLANCHOT, Georges (CERN); BONNAUD, Julien (CERN); KOVACS, Mark Istvan (CERN); GAJANEC, Rafael (Slovak Technical University (SK))

Presenter: GADEK, Tomasz (CERN)

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