Contribution ID: **132** Type: **Poster**

The WaveCatcher systems: a family of powerful and low cost digitizers.

Thursday 20 September 2018 17:00 (15 minutes)

The WaveCatcher systems are a family of powerful and low cost digitizers. Their number of channels ranges between 2 and 64. They easily replace oscilloscopes in numerous applications. They are based on the SAMLONG ASIC which samples the signal between 400 MS/s and 3.2 GS/s over 12 bits with a bandwidth of 500 MHz.
The systems can also be used as TDCs for high precision time measurement. Sampling time precision after calibration is indeed better than 5 ps rms at 3.2GS/s. They house USB and secured Gbit-UDP interfaces. A powerful software and a complete C library are also available.

Summary

Introduced at TWEPP in 2009, the WaveCatcher boards and modules are 12-bit 3.2 GS/s Switched Capacitor Digitizers issued from the collaboration between CEA/IRFU & CNRS/IN2P3/LAL and based on the SAMLONG chip, developed on the basis of a common patent.
The input dynamic range is 2.5 Vpp (DC coupled), with individual DC offset adjustable in the ±1.25V range via a 16-bit DAC. The signal bandwidth is 500 MHz @3dB.
The input signals are continuously sampled inside the SAMLONG chips in a circular analog memory buffer (1024 cells) at a frequency selectable between 0.4 and 3.2 GS/s. As a trigger signal arrives, all analog memory buffers are frozen and subsequently digitized with a resolution of 12 bits. Up to 7 full events per channel (1 event = 1024 words of 12 bits) can be stored consecutively. During conversion process, the WaveCatcher cannot handle other triggers, and thus generates a dead time (maximum 125 µs, decreasing proportionally with the recording depth thanks to the configurable record length).
Each input channel is equipped with a discriminator using a 16-bit programmable threshold, which generates trigger primitives. Primitives from all channels are processed by the board to generate a common trigger causing all the channels to acquire an event simultaneously. This common board trigger can be based on any combination (including multiplicity) of the channel discriminators and/or the external trigger.
Each pair of channels is equipped with a 40-bit TDC (counter) tagging the trigger with the clock delivered to the SAMLONG chips (200 MHz down to 25 MHz depending on the selected sampling frequency).
Each input channel is equipped with a programmable hit rate monitor based on its own discriminator and on two counters giving the number of hits which crossed the programmed discriminator threshold (also during the dead time period) and the time elapsed. This permits measuring the hit rates independently of event readout.
Each input channel is also equipped with a digital measurement block located in the front-end FPGA which permits extracting in real time all the main features from the signal: baseline, peak, charge, time of the edges in CFD or fixed threshold modes. These measurements can be sent together with the waveforms or in standalone.
The module supports multi-board synchronization allowing all SAMLONG chips to be synchronized with a common clock source and ensuring triggering them in phase. All data will then be aligned and coherent between multiple WaveCatcher boards.
All WaveCatchers house USB 2.0 which allows data transfers up to 30 MB/s. The 8-channel module and 64-channel crate also provide a secured Gbit-UDP interface. In addition, all the boards house a secured Gbit-UDP

Optical Link.
Considering the performance of the modules, they are well suited and widely used for very fast signals as those generated by fast scintillators or crystals coupled to PMTs, MCP-PMTs, Silicon Photomultipliers, APDs, Diamond detectors,…
A new version of SAMLONG will be submitted in May 2018. It should permit increasing the ADC range up to 14 bits, while keeping or even improving all the other performance parameters.

Authors: Mr BRETON, Dominique (CNRS/LAL Orsay (FR)); Mr DELAGNES, Eric (CEA); Mrs MAALMI, Jihane (CNRS/LAL Orsay (FR))

Co-author: Mr RUSQUART, Pascal (CNRS/LAL Orsay (FR))

Presenter: Mr BRETON, Dominique (CNRS/LAL Orsay (FR))

Session Classification: Posters

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience