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CMS ECAL Upgrade Front End card: design and prototype test results

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CMS ECAL Phase2 Front-End(FE) card is designed to provide streaming of the data generated on the Very-Frond-End(VFE) cards to the back-end electronics. FE card will use the components developed within the VersatileLink project. It will contain four or six lpGBT ASICS with corresponding VersatileLink+ optical modules. Prototype FE card was developed to validate the clock distribution, high speed data links and other technical features of the future design using the currently available GBT and VersatileLink components.
The current version of the upgrade FE card design will be discussed as well as the design and test results of the GBT-based prototype.

Summary

The primary driver of the ECAL barrel calorimeter upgrade is the trigger requirements for a trigger latency of 12.5 ms and a Level 1 trigger rate of 750 kHz.
The proposed solution –stream all data generated on Very-Front-End (VFE) cards off-detector to Barrel Calorimeter Processor (BCP). This will allow to make all trigger-related calculations and decisions off-detector and granulation and trigger latency will depend on the BCP processing power, which can be easily upgraded later with arrival of more powerful processors.
The legacy VFE generate 14 bits information per calorimeter channel (crystal) at 40MHz rate. Which results to the 14Gb/s data rate for each FE card, serving to stream the data from one Trigger Tower (5x5 crystals). This data rate can be handled by five GBTx transmitters, each providing 3.36Gb/s user data rate.
The upgrade VFE card will run at 160MHz sampling to coop with the high pileup and provide much better time resolution. The ECAL barrel detector elements, crystals and APDs, allow this improvement, as it was shown by the realistic tests, including ones with the beam.
Hence, the target FE data transmission rate is 13bits@160Mhs x 25 channels per tower –52Gb/s. To coop with such rate we should first, use the next generation rad. tolerant data encoders, lpGBT, running at 10Gb/s, and second, apply some data reduction / compression procedure at VFE level.
Since the design and implementation of VFE on-board data compression is not yest completed, we design two versions of the FE card with four and six lpGBT and Versatile Link Plus (VL+) transmitters for compression / no compression options.
The current state of the design will be presented and discussed.
The lpGBT and VL+ components are not currently available for users. Hence the first version of FE prototype is built with the currently available GBT components: GBTx, GBT-SCA and VL transceivers. The FE Prototype0 contain five data transmission channels and has sufficient capacity to stream the data of the legacy VFE card. This prototype also allows to test of the precision clock distribution and slow control via optical downlink. We used in the design the features of GBTx which is supposed to be common with the future lpGBT.
The details of the Prototype0 design and results of the laboratory and beam tests will be discussed.

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