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ATLAS Phase-II-Upgrade Pixel Demonstrator Read-out

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The ATLAS tracking system will be replaced by an all-silicon detector (ITk) in the course of the HL-LHC upgrade around 2025. The read-out of the ITk pixel system will be most challenging in terms of data rate. First test of read-out concepts are performed with the ITk Pixel "demonstrator", a system composed of several ITk-style modules with in total 120 FE-I4 read-out chips. Their read-out is realised with data aggregation via GBTx chips transmitting data optically to "Cluster On Board"(COB) ATCA-boards acting as off-detector components. The system layout and first test results will be presented.

Summary

ATLAS is preparing for an extensive modification of its detector in the course of the planned HL-LHC accelerator upgrade around 2025 which includes a replacement of the entire tracking system by an all-silicon detector (Inner Tracker, ITk) and a revised trigger and data taking system. The five innermost layers of ITk will comprise of a pixel detector. The readout of the pixel layers will be most challenging in terms of data rate and read-out speed (up to 5.12 Gb/s per link) and in terms of number of modules to handle –approx. a factor of 10 more compared to the current ATLAS Pixel Detector.
Even though the final on-detector electronics is not yet available, initial system test measurements were performed based on the legacy read-out chip FE-I4 and read-out systems developed further from their applications during construction of the Insertable B-Layer (IBL) of the current Pixel Detector to test ITk-specific DAQ aspects. The Demonstrator Project offers a test bench in terms of on-detector electronics. A local support structure is equipped with fully functional FE-I4 modules in ITk-style and powered and read out with services as close a possible to ITk designs. This system comprises of a total of 120 FE-I4 chips. At the end of the structure, all electrical links are connected to several Versatile Link Demo Boards (VLDB) or alternatively to a custom-made PCB hosting several GBTx chips identical to those used on the VLDB. The GBTx aggregates uplinks and disentangles aggregated downlink data of up to 20 FE-I4 and communicates to off-detector electronics over a fibre pair at 4.8 Gb/s using the GBT protocol. One of the employed off-detector electronics options is the ATCA-based RCE read-out system consisting of a COB (cluster on board) ATCA carrier board, a DPM (data processing module), a DTM (data transportation module), and an RTM (Rear Transition Module) containing SFP+ transceivers. 3 DPMs out of the 4 available DPMs on the COB are needed to read out the 120 FE-I4 front-ends on the Demonstrator structure. In addition to the GBT firmware the RCE contains formatting for the FE-I4 data. The data are then transferred via DMA to the ARM processor on the RCE where the calibration loops run and where results get histogrammed. The scan is controlled through a GUI that runs on a Linux server. The GUI also reads back the histograms from the RCE and performs analysis. The communication between the server and the RCE is done via ethernet (1 or 10 Gb/s). All the common calibration scans are implemented since the RCE system was used for the IBL stave QA. The status of the GBTx-based read-out with RCE and first test measurements with several demonstrator modules are presented.

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