The CMS phase 2 ECAL front end electronics upgrade

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The CMS ECAL barrel electronics will be upgraded for the HL-LHC to comply with increased latency and bandwidth requirements of the Level 1 trigger, to preserve detector performance despite the increased instantaneous luminosity, and to provide a precision timing measurement in addition to energy. The chosen solution includes a custom dual gain trans-impedance amplifier implemented in a 130 nm CMOS process and a dual ADC ASIC implementing gain selection and data compression implemented in a 65 nm CMOS process.

ECAL Barrel electronics

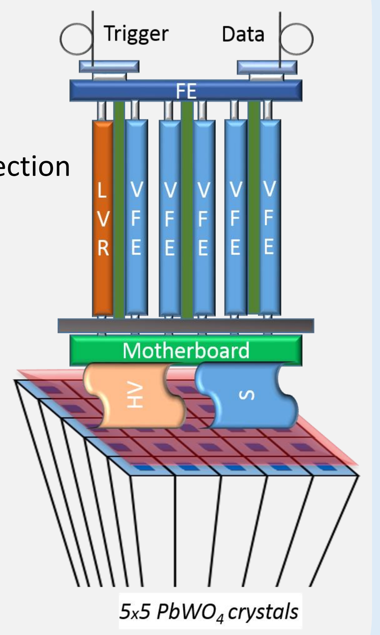
1 Module called "Trigger Tower":
- Readout of 5x5 crystals matrix.
- Each crystal has 2 APDs glued, connected in parallel

❑ **Motherboard:**
- Passive board used to provide HV for APDs and VFE inputs connection

❑ **Very Front End (VFE):**
- 5 cards / module
- Each VFE has 5 identical readout channels with pre-amplifier (MGPA), filter and 12-bit ADC

❑ **Front-end card (FE):**
- This card generates trigger data summing of 5x5 crystal signals and has latency buffer (< 6μs) to store data while waiting for L1 accept.
- The readout between data & trigger is separated.
- 40 MHz readout of the tower
- 100 kHz readout of single crystals for triggered events

❑ **Low Voltage Regulator card (LVR):**
- 10 linear radiation tolerant regulators



CMS Barrel ECAL upgrade at HL-LHC

Extraction and refurbishment of the 36 EB Super modules during LS3

❑ **Replace FE and VFE cards:**
- To be compatible with increased Phase II trigger requirements
- To cope with challenging HL-LHC conditions

(noise, PU, anomalous APD signals) keeping the dynamic range
- To increase the time measurement resolution for high energy photons

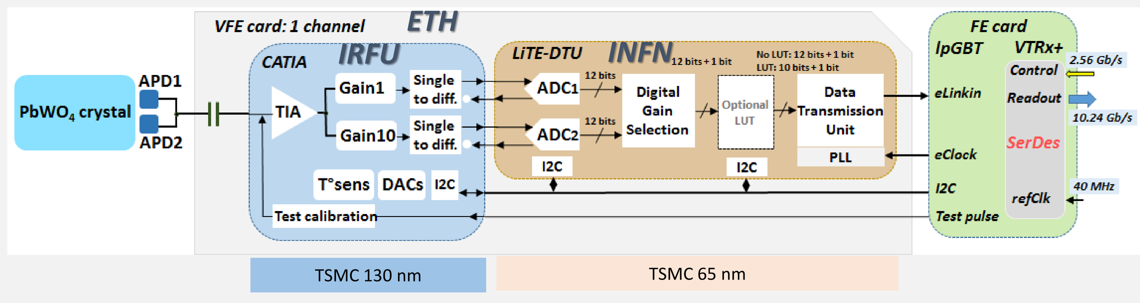
❑ **Reduce temperature from 18° C to 8° C:**
- To mitigate the increase of APD dark current with the radiation

❑ **Off-detector electronics upgraded to:**
- Higher transfer rates
- Generation of trigger primitives

❑ **SLVR card:**
- DCDC radiation + magnetic field tolerant

❑ ***$PbWO_4$ crystals, APDs, Motherboards & overall mechanical structure will remain***

CMS Barrel ECAL VFE upgrade: TIA + Fast ADC



❑ **CATIA** (**CA**lorimeter **T**rans **I**mpedance **A**mplifier) ASIC:
- **TIA** & 2 Gain stages (G1, G10); Test calibration; T° sensor; I2C

❑ **LiTE-DTU** (**Li**sbon-**T**orino **E**CAL **D**ata **T**ransmission **U**nit) ASIC:
- 12-bit ADC, 160 MHz sampling, dual channel with gain selection logic: **IP** from external supplier
- Data Transmission Unit (DTU) implements data compression before FE

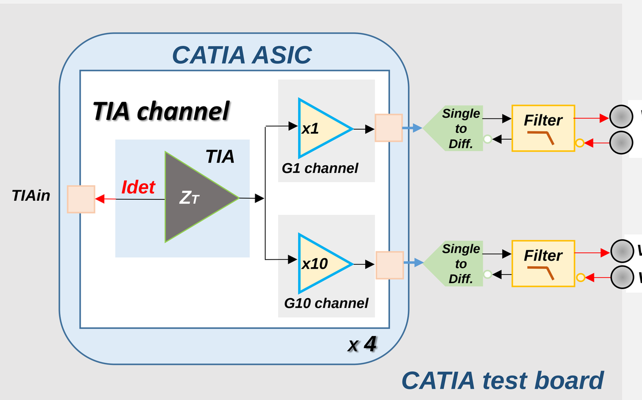
❑ **FE:**
- lpGBT (4x10.24 Gb/s data links, 1x2.56 Gb/s control link)
- eLink serial interface to ADC, clock and I2C interface

❑ **Low Voltage Regulator (LVR):**
- needed voltages (1.2V & 2.5V) supplied by point-of-load FEAST DC/DC converters

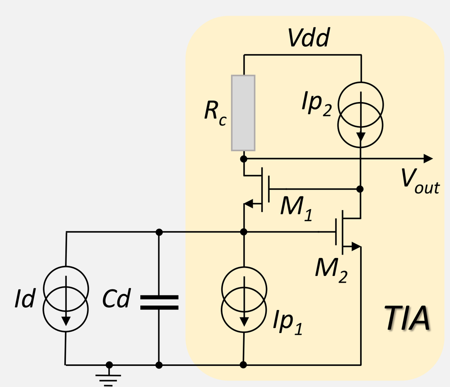
CATIA V0 : main features

❑ **First prototype**
- **Proof of concept** : TIA instead of CSA (legacy architecture)
- **Transistors flavor** selection **(1.2V or 2.5V)**
- Full characterization **with detectors**

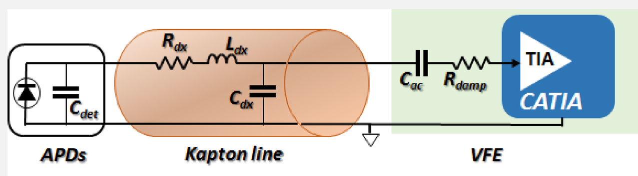
CATIA V0
- Process: TSMC 130 nm
- 2352μm x 3323μm
- LQFP 100L 14x14
- Test: 2017

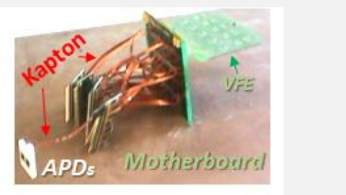


CATIA architecture
- **1 channel** = TIA + 2 Gains (G1, G10)
- **4 TIA channels** with different gain architectures and voltage supply (1.2 thin oxide & 2.5 V thick oxide)
- **Filter** is outside of the chip for bandwidth tuning



TIA architecture
- **Regulated Common-Gate** (RCG): low Z_{in} (< 1 Ω) compatible with 50 MHz of bandwidth for C_d = 200 pF



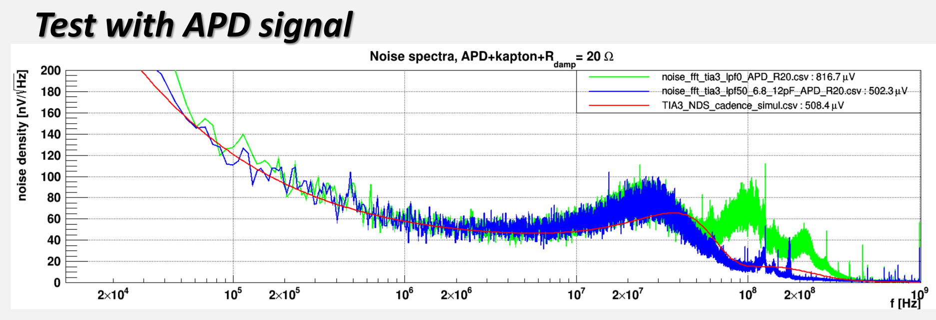


Kapton line parameters:
R_{dx} = 0.05 Ω / cm
L_{dx} = 3.75 nH / cm
C_{dx} = 2.4 pF / cm
Length: ≈ 20 cm

APD to TIA input: strip lines
High value of inductance (75 to 100 nH):
Need damping resistor to ensure stability
=> Impact on the BW, timing & charge resolution

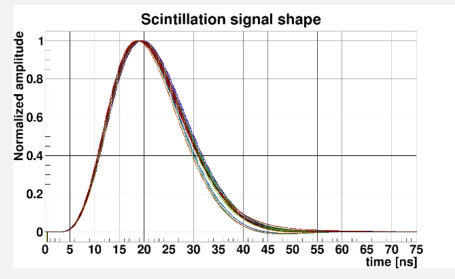
CATIA V0 : test results summary[1]

Test with APD signal



Noise density spectra of CATIA connected to APDs as in ECAL.
In green, without bandwidth limitations,
in blue with a low pass filter at 50 MHz and
in red the simulation results

Test-beam



H4 Test-beam April 2018
Response of 15 crystals:
CATIA-V0 + 14-bit ADC 160 MS/s

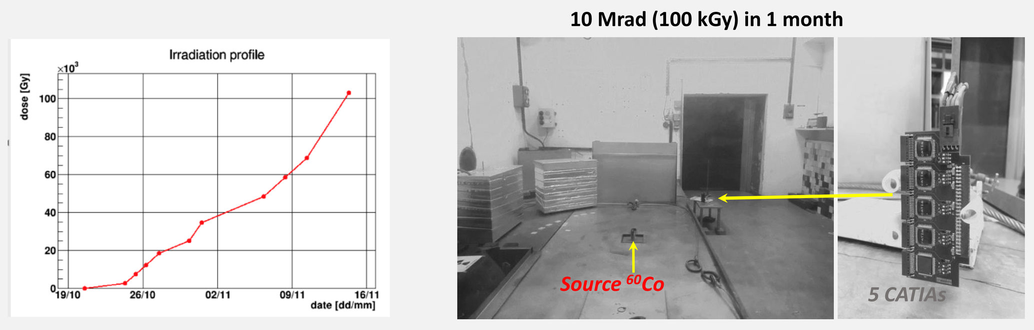
- The test results are very consistent with simulation results
- For the final version, it will be interesting to choose the thick oxide transistors (2.5 V):
- Advantages: better dynamic range, linearity and noise performances
- **But thick oxide is expected to be less tolerant to radiation** (expected 1 Mrad, required tolerance > 10 Mrad)

⇒ **radiation test mandatory**

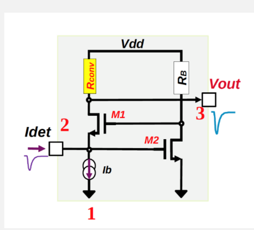
[1]For more test results see poster TWEPP 2017

Irradiation tests

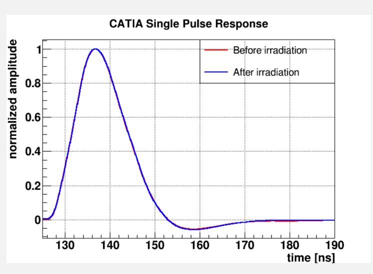
- Irradiation at *Pagure* in 2017: CEA-Saclay facility



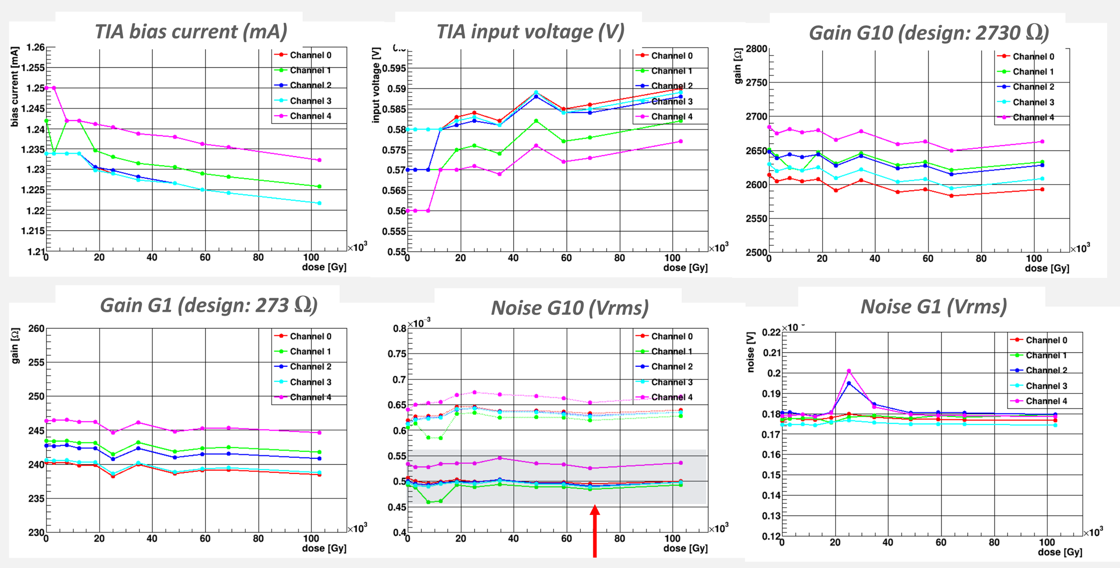
❑**Test 1.2V and 2.5V versions on 5 prototypes**
- Power supplies current
- TIA bias current (1), TIA input voltage (2)
- TIA output voltage for G1 and G10 (3)
- Noise, Gain-linearity, Bandwidth, rise time



❑**Transient response with detector:**
- 10 Mrad
- TIA 2.5 V
- G1

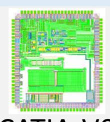


❑**2.5V thick oxide TIA results:**



❑**Conclusions**
- Radiation hardness test shows that the 2.5V thick oxide CATIA version meets the radiation hardness requirements for CMS ECAL barrel and is selected as the baseline for the **CATIA V1**

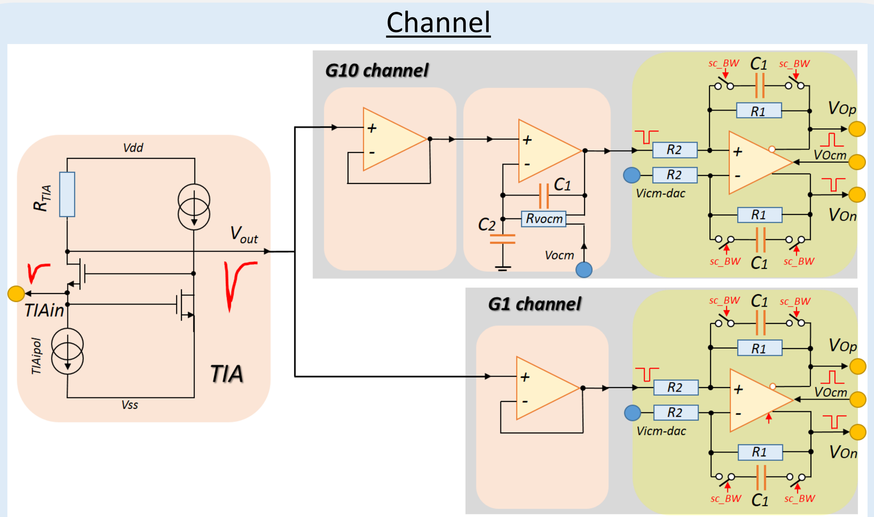
CATIA V1



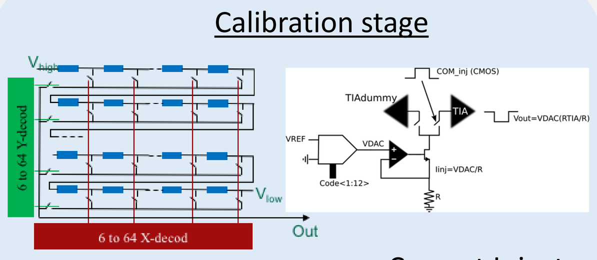
❑ Based on current amplifier TIA used in CATIA-V0
❑ 2 differential voltage outputs covering 2 input dynamic charge ranges: 10 MeV-200 GeV & 10 MeV-2 TeV
❑ Must be interfaced with 12-bit ADC: +/- 0.6 V per input; Vicm = 0.6V
❑ Output pedestal adjusted through internal threshold adjustments (5-bit DAC)
❑ Integrated Filter to control the bandwidth of the analog signal processing
❑ Calibration system with 2/1000 of precision (12 bits current source)
❑ I2C with TMR for slow control (gain, bandwidth, calibration…)
❑ Temperature sensor (-40=>+80°C, 1.3mV/°C) based on CERN Bandgap
❑ Technology: 130 nm TSMC; 1.2 & 2.5 V

Architecture

Channel



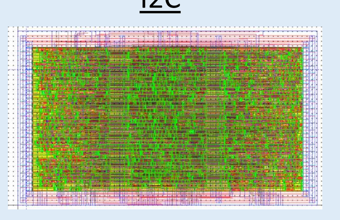
Calibration stage



12-bits DAC
R ladder with XY addressing
=>low power & high linearity.

Current Injector

I2C



310 x 180 μm² with 64 bits register
Full TMR, event driven (no ext. clock)
7 bit address, all I2C speed mode

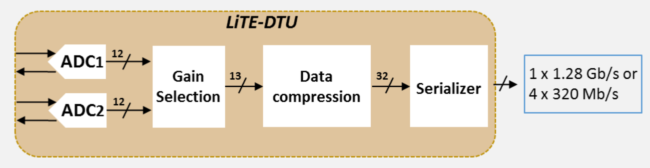
Simulation results

luminosity	ileak	E Resolution; η = 0	T Resolution @ 50 GeV; η = 0	ileak	E Resolution; η = 1.45	T Resolution @ 50 GeV; η = 1.45
300 fb-1	5 μA	105 MeV	15 ps	10 μA	135 MeV	21 ps
4500 fb-1	80 μA	380 MeV	57 ps	140 μA	890 MeV	134 ps

Submitted in July 2018 => test results before 2019.

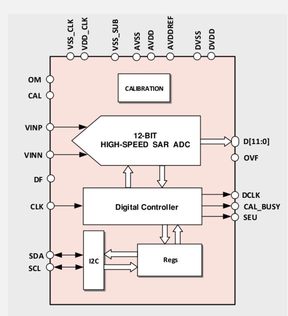
LiTE-DTU Architecture

❑ ***ADC***
IP provided by S3 Group guided by LIP
❑ **ASIC** integration by INFN.
❑ ***DTU***
Data compression and Transmission at 1 x 1.28 Gb/s or 4x320 Mb/s



ADC requirements

Specification	min	typ	max	unit
Sampling rate	160			MS/s
Resolution	12			bit
Supply voltage	1.08	1.2	1.32	V
Differential input range		± 0.6		V
DNL			± 0.9	LSB
INL			± 1.5	LSB
Operational temperature	-20	25	85	°C
Power consumption		20		mW
Latency		15		T_{CK}
Calibration time			38200	T_{CK}
Technology	CMOS 65 nm (9+1 metal stack)			
TID tolerance	20			kGy
SEU tolerance	15			MeV cm²/mg

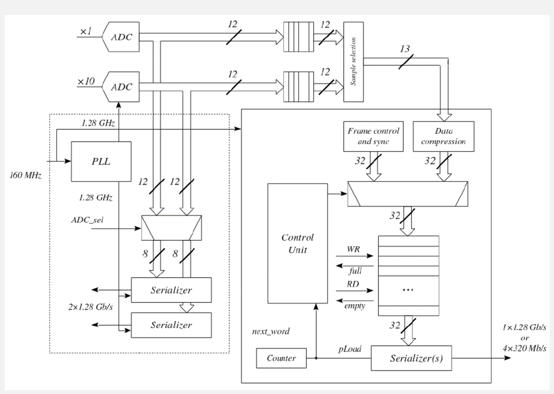


❑ ***ADC IP block***
- ➢ This ADC is based on original ADC designed in 40 nm technology
- ➢ Time Interleaved dual core architecture.
- ➢ Each core 12bits, 80 MS/s SAR ADC
- ➢ TMR on control logic and RD53-based design guidelines (for TID tolerance)
- ➢ Delivery of full gdsII: September 2018

DTU architecture

❑ ***Data compression***
- ➢ Word size 32 bits in order to minimize the BW for baseline samples (< 7 bits)
- ➢ Total bandwidth without compression: 160 MS/s x 13 bits = 2.08 Gb/s
- ➢ Probability to have an event with more than 6 bits < $2.37\ 10^{-4}$
- ➢ Baseline rate: 160 MS/s x (1-2.37 10^{-4}) x 32/5 = 1.024 Gb/s
- ➢ Signal rate: 160 MS/s x 2.37 10^{-4} x 32/2 = 0.61 Mb/s
- ➢ Baseline rate close to signal: 160 MS/s x 2.37 10^{-4} x 32 = 1.22 Mb/s
- ➢ Protocol overhead (estimated): 50 Mb/s

❑ ***Bandwidth comparison & Readout options***
- Total bandwidth required per channel 1.08 Gb/s
- Total bandwidth available: 1.28 Gb/s (distributed over 1, 2 or 4 e-links)



Submission: November 2018.

Conclusion

❑ The ECAL Barrel VFE must be redesigned for the upgrade phase II
❑ The new VFE architecture will be faster by using **TIA** coupled with **ADC 160 MS/s**
❑ Submission & test including radiation hardness (TID) of the first prototype CATIA-V0 permit to validate the choice of this solution for ECAL at HL-LHC. The new version **CATIA-V1** is more complete and compatible with the 12-bit ADC chosen also for ECAL VFE. The ASIC has been submitted the 4th of July 2018 and will be tested before end 2018. Some news hopefully at TWEPP 2019.
❑ The first prototype of 12-bit ADC will be provided by S3 in September 2018. The first complete LiTE-DTU will be submitted in November 2018.

TWEPP 2018: Topical Workshop on Electronics for Particle Physics 17-21 September 2018, Antwerpen