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The CMS phase 2 ECAL front end electronics upgrade

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The CMS ECAL barrel electronics will be upgraded for the HL-LHC to comply with increased latency and bandwidth requirements of the Level 1 trigger, to preserve detector performance despite the increased instantaneous luminosity, and to provide a precision timing measurement in addition to energy. The chosen solution includes a custom dual gain trans-impedance amplifier implemented in a 130nm CMOS process and a dual ADC ASIC implementing gain selection and data compression implemented in a 65nm CMOS process. Test results and the development plan for the CMS ECAL barrel front end electronics system up to installation readiness will be presented.

Summary

The Compact Muon Solenoid (CMS) experiment was designed to record highest quality experimental data for 10 years and for an integrated luminosity of 500 fb-1 at a peak rate of 1*1034 cm-2s-1. During the High Luminosity LHC (HL-LHC) era the LHC will deliver an additional 3000 or even 4000 fb-1 of integrated luminosity at a levelled peak rate of* 71034 cm-2, thus allow recording one order of magnitude of additional data for analysis.
The CMS collaboration will modify the experiment in order to:
• cope effectively with the higher hit density (in time pile up)
• cope effectively with the higher hit rate (out of time pile up)
• maintain availability through the extended operating period
• maintain data quality, thus limit the degradation due to aging and radiation damage
• improve the selectivity of the trigger system
• increase the capacity of the readout system
The level 1 trigger has to select events at high efficiency within a limited latency under the HL-LHC conditions. CMS has decided to limit the level 1 trigger latency to 12.5 microseconds to be compared to 3.2 microseconds for the legacy system.
The central data acquisition system has to have the capacity to read out data at a higher rate than for the legacy experiment. CMS has decided that the trigger rate should be below 750 kHz. Taking the increase in event size due to new and more granular detectors into account the data acquisition system will have to increase the capacity by two orders of magnitude compared to legacy.
The main motivation for the ECAL barrel electronics system upgrade are the two last point mentioned above; The readout rate of the legacy system can't exceed 130kHz and the granularity of the legacy trigger primitive generator is defined by rigid clusters of five by five crystals forming a trigger tower. Moving the primary event buffers outside the experiment and into the back-end electronics system addresses the DAQ readout rate issue. Streaming the crystal data from the front end allows full flexibility in the formation of the trigger primitives.
The new front-end electronics system is designed to mitigate the due to radiation damage increasing noise from the avalanche photodiodes (APDs), to discriminate anomalous APD signals and to provide improved timing information. The implemented solution is a Trans-Impedance Amplifier ASIC (TIA, named CATIA) coupled with a digitizer ASIC (LiTE-DTU).
CATIA provides two analogue outputs with different gain, both with the bandwidth required to maintain the

precision of the detector signal. CATIA is integrating the findings of the first prototype which was implemented in TSMC 130 nm CMOS technology. CATIA feeds the two analogue signals to LiTE-DTU, a dual 12 bit ADC sampling at 160 MS/s. LiTE-DTU integrates two ADCs, logic for gain selection, and a data compression stage. The ADC IP core development has been outsourced to an external supplier, a procedure analogue to the one employed for the development of the ADC chip used in the current CMS ECAL.

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