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ATLAS Phase-II-Upgrade Pixel Data Transmission Development

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The ATLAS tracking system will be replaced by an all-silicon detector (ITk) in the course of the HL-LHC upgrade around 2025. The readout of the ITk pixel system will be most challenging in terms of data rate. Simulation of the on-detector electronics based on a trigger rate of 1 MHz indicate that a readout speed of up to 5 Gbps per data link is necessary. Due to radiation levels, the first part of transmission is implemented electrically, realised by "active cables"integrating data aggregator and equalizer ASICs. The system layout and updates on simulation and test results will be presented.

Summary

ATLAS is preparing for an extensive modification of its detector in the course of the planned HL-LHC accelerator upgrade around 2025 which includes a replacement of the entire tracking system by an all-silicon detector (Inner Tracker, ITk) and a revised trigger and data taking system with triggers expected at lowest level at an average rate of 1 MHz. The five innermost layers of ITk will comprise of a pixel detector. The readout of the pixel layers will be most challenging in terms of data rate and readout speed. A first prototype of the new on-detector readout chip was designed in the context of the RD53 Collaboration which will serve as a basis for the final chip. The performance of the readout system was simulated based on hit rates from detector simulation combined with behavior expected from the current chip design with proposed modifications, assuming different data formats and possible compression methods with proposed trigger parameters. This simulation indicates that the expected maximum combined readout speed of 5.12 Gb/s of the four chip differential drivers will be consumed in the innermost layers. The readout speed per chip is going down to values well below 1 Gb/s in the outermost layers. Up- and downlink communication to the on-detector electronics is foreseen to be largely optical and expected to be realized with components from the VersatileLink+ project. However, radiation levels close to the beam pipe prevent the placement of optical components close to the readout chips such that the first part of transmission has to be implemented electrically with signals to be converted for optical transmission at larger radii. Options to aggregate data links of one chip in the innermost layer and of several chips on one module of outer layers are developed in order to provide the required bandwidth while reducing needed material. Aggregation will be realized in a dedicated ASIC in conjunction with cables suited for electrical data transmission at rates of up to 5 Gb/s over several meters. Aggregation on the uplinks will be based on the Aurora protocol used by the readout chip, while downlinks will be aggregated on the off-detector side using the GBT protocol. Both approaches are compatible with the ATLAS-wide generic off-detector FELIX readout concept. Designs of the electrical links cover solutions such as twin-axial or twisted pair cables. Prototype cable attenuation behavior derived from simulation, S-parameter analysis and eye-diagram inspection demonstrate the need for equalization which will be realized as another ASIC on the optical component side of the cable. The status of concepts for the two additional ASICs, cable candidates with recent test results, their integration as "active cable"and their connection to the RD53-style readout chip as well as the optical components and the FELIX off-detector system, and the performance in the entire readout chain based on simulations will be presented.

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