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Electronics Developments for Phase-2 Upgrade of CMS Drift Tubes

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Considerable enhancements are foreseen for the Drift Tubes (DT) subdetector during Phase-2 CMS upgrade. The new HL-LHC CMS Trigger/DAQ requirements exceed the present capabilities of the on detector electronics (MiniCrate). Therefore, as a consequence of the higher L1A rate set by CMS, as well as MiniCrate maintainability and chamber aging mitigation arguments, all MiniCrates will be replaced during LS3. The phase-2 on detector electronics for DT will consist of only a single type of board called OBDT (On Board electronics for Drift Tubes). A description of it will be given along with the status of the prototype and validation tests.

Summary

Considerable enhancements are foreseen for the Drift Tubes (DT) subdetector during Phase-2 CMS upgrade. The new HL-LHC CMS Trigger/DAQ requirements exceed the present capabilities of the on detector electronics (MiniCrate) in terms of Level 1 trigger accept rate. Therefore, as a consequence of the higher L1A rate set by CMS, as well as MiniCrate maintainability and chamber aging mitigation arguments, all MiniCrates together with the associated back-end electronics will be replaced during LS3. The partitioning of the electronics components between UXC and USC will be re-optimized making use of the higher bandwidth optical link technologies available at low cost now. The main goal of the new electronics will be to allow more performing DT trigger algorithms that mitigates chamber aging effects and that match better with the new information made available in Phase-2 from the new tracker. HLT resolution will made available at L1 trigger and deadtime will be reduced to the minimum achievable by the present chamber. Another goal of the new on detector electronics is to get a more maintainable system. The present MiniCrate is a complex system involving many different kinds of boards with several ASICs dated back to the 90s and it is not guarantee its reliability can be extended after LS3. The phase-2 on detector electronics for DT will consist of only a single type of board called OBDT (On Board electronics for Drift Tubes). The OBDT receives signal hits from each analog FE chip and assigns a digital timestamp. It hosts a multi-channel TDC implemented in a radiation hard FPGA and its associated services. The data are transferred out of the experimental cavern using CERN developed high bandwidth optical link technology. Readout pipeline buffering and trigger primitive generation will be done in boards located outside the experimental cavern profiting from the more relaxed environmental constraints. A prototype of the OBDT is going to be produced and tested in 2018. Such prototype will be centered around a Microsemi PolarFire flash-based FPGA able to host 240 TDCs with the ns resolution. The timing and slow control distribution will be done by the GBT chipset while the data transfer will be performed directly through the fast serializers of the FPGA able to reach a transfer rate greater than 10Gbps. A full description of the OBDT will be given along with the status of the prototype production and validation tests.

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