Flexible Printed Circuit design and testing for the High-Granularity Timing Detector for the Phase II upgrade of the ATLAS calorimeter system

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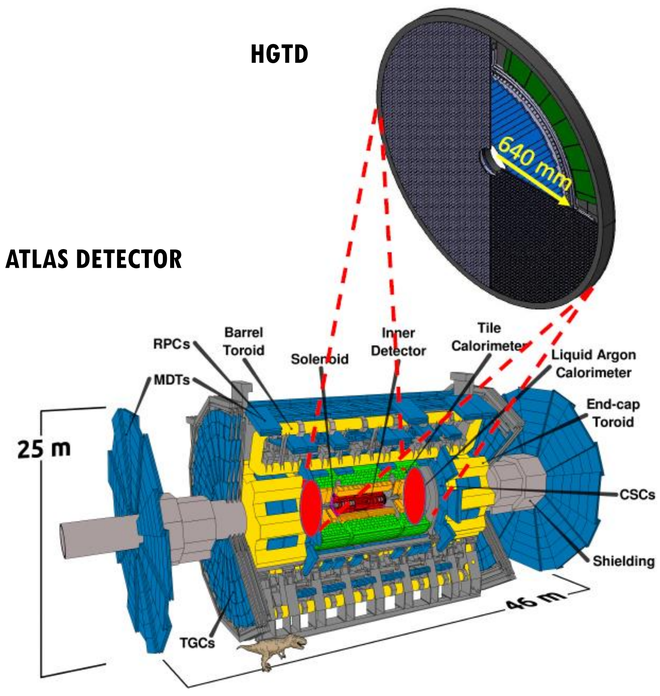
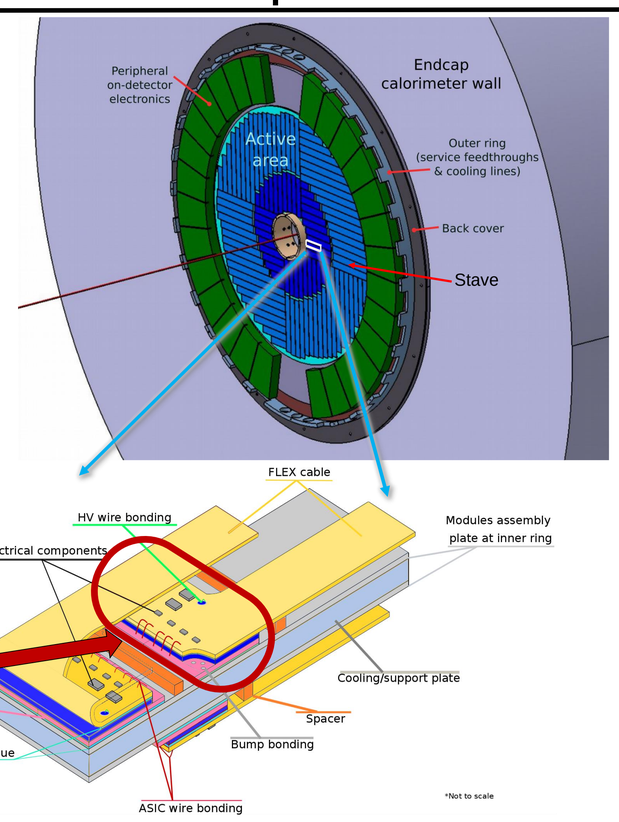
High-Granularity Timing Detector (HGTD)



The High-Granularity Timing Detector (HGTD) will improve the performance of the ATLAS detector (in the endcap and forward regions) for Phase II upgrade in the HL-LHC by providing 30 ps time resolution. The detector base unit consists of a hybrid module of 2x4 cm^2 Low Gain Avalanche Detector (LGAD) bump-bonded to two ASICs and wire-bonded to a Flexible Printed circuit (FLEX cable)

Basic detector unit: module
A module consists of a LGAD + 2 ASICs + FLEX cable



Electrical requirements per module

Signal type	Signal name	No. of wires	Comments
HV	1 kV max.	2	Clearance
POWER	1x Vdda, 1x Vddd	2	Minimise voltage drop
GROUND	Analog, Digital	1 plane	Dedicated layer
Slow control	Data, Ck (opt. +rst, error)	2 to 4	I2C link
Input clocks	320 MHz, Fast command e-link	6 or 8	LVDS
Data out lines	Readout data (TOT, TOA, Lumi)	4 pairs	4 e-links differential SLVS
ASIC reset	ASIC_rst	1	Digital
Temperature	ASIC_temperature	2	DC voltage
DC/DC power	DCDC _pwr	2 or 3	Sense signals of DC/DC

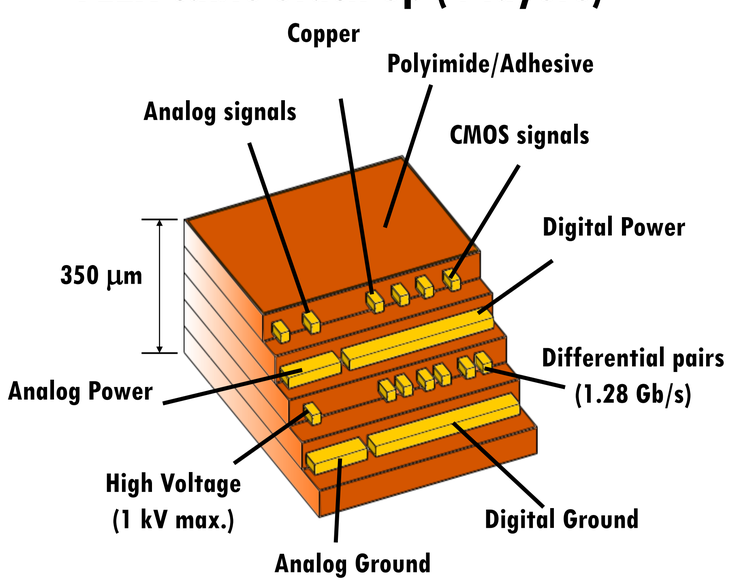
Why a Flexible Printed Circuit (FPC)?

Very strict mechanical constraints make a FPC the most suitable candidate to connect the the electrical signals between the modules and the peripheral on-detector electronics

Mechanical constraints

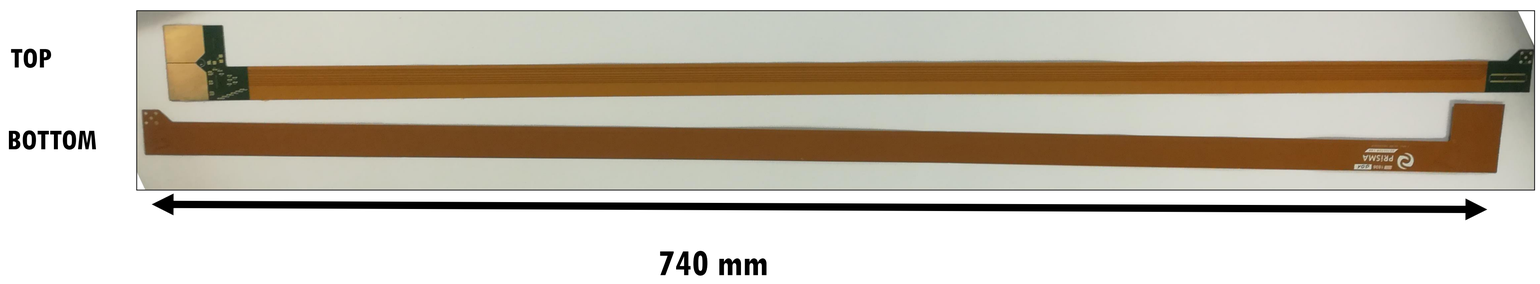
Distance of the innermost module to the start of the peripheral on-detector boards is 630 mm → maximum **length of 740 mm**
Width < 19 mm two co-planar FLEX cables with half the size to reduce the total thickness
Thickness < 350 μm to fit within the available space height of the stave

FLEX cable stack up (4 layers)



FLEX cable prototype

The prototype is in a study phase to understand the technology requirements (materials, manufacturing capability, electrical and mechanical robustness) and to address the potential problems by representing a significant subset of the signals (signal integrity, power distribution, HV-insulation, interference and crosstalk).



Power Integrity Simulations

Post-layout simulations with Cadence "Sigrity" and "PowerSI" [1] (signal integrity and power distribution over long lines)

The result of this simulation is fundamental since the signal integrity can be affected by any power instability

Comparison between the resistance of the hatched and non-hatched geometry for power and ground planes. The current prototype has hatched planes (Ratio = $R_{hatched}/R_{non\text{-}hatched}$)

A 4x higher resistance is tolerated in the power distribution to accomplish the better matching on the transmission line impedance (Signal Wave Ratio > 5:1). If lab tests present larger values, sense lines will be included to fully compensate the voltage drop

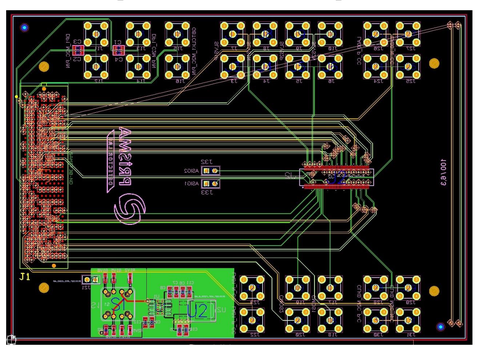
Simulation results

Plane	Ratio
Power analog	3.51
Power digital	4.57
Ground analog	3.60
Ground digital	4.50

Test plan

- An adapter board has been developed as plug-in for the FMC High-Speed connector on the Kintex KC705 [2].
- The FPGA is programmed to inject test patterns at **1.28 Gb/s** and check the response with the **IBERT**. SMA connectors on the adapter board route the signals to the oscilloscope for classical eye-diagram analysis.

Adapter board layout



- The I/O drivers in the KC705 are compatible with the VC707[3] used by the LpGBT [4] designers. Test conditions close to the on-field operation.
- The **insulation** of the FLEX materials is checked up to 1 kV with the **Megger MIT430 tester** [5] . The IBERT will be tested w/wo HV
- **Time Domain Reflectrometry (TDR)** in order to check the impedance homogeneity of the tracks. Crucial for high-speed data transmission.
- The test plan is performed at both room temperature and -30°C, required to decrease the leakage current when running the sensors, to reproduce the temperature conditions in the HGTD.

[1] Cadence Sigrity and PowerSI Cadence Desgn Systems Inc, https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/pcb-design-analysis/sigrity-powersi-ds.pdf
[2] K7C05 Evaluation Board. Xilink Inc. https://www.xilinx.com/support/documentation/boards_and_kits/kc705/ug810_KC705_Eval_Bd.pdf
[3] VC707 Evaluation Board. Xilink Inc. https://www.xilinx.com/support/documentation/boards_and_kits/vc707/ug885_VC707_Eval_Bd.pdf
[4] LpGBT project. GBT project "Radiation Hard Optical Link Project". https://espace.cern.ch/GBT-Project/default.aspx
[5] CAT IV Insulation teter MIT400/2 series https://megger.com/cat-iv-insulation-testers-mit400/2-series

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