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Level-1 Data Driver Card - A high bandwidth radiation tolerant aggregator board for detectors

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The Level-1 Data Driver Card (L1DDC) was designed for the needs of the future upgrades of the innermost stations of the ATLAS end-cap muon spectrometer. L1DDC is a high speed aggregator board capable of communicating with multiple front-end electronic boards. It collects the Level-1 data along with monitoring data and transmits them to a network interface through bidirectional and/or unidirectional fiber links at 4.8 Gbps each and distributes trigger, time and configuration data coming from the network interface to the front-end boards.
In this paper, the L1DDC boards will be described and the results from radiation tests will be presented.

Summary

The Level-1 Data Driver Card (L1DDC) was designed for the needs of the future upgrades of the innermost stations of the ATLAS end-cap muon spectrometer at LHC. The detectors located at the muon Small Wheels will be replaced by a set of precision tracking and trigger detectors, the resistive Micromegas (MM) and the small-strip Thin Gap Chambers (sTGC). After the upgrade, the number of interactions per bunch crossing will be increased up to 140, resulting in a dramatically large amount of produced data. The high number of electronic channels (about two million for the MM and about 300k for the sTGC) along with a harsh environment (radiation dose up to 1700Gy (inner radius) and a magnetic field up to 0.4T in the end cap region) led to the development of new radiation tolerant electronics and a scalable readout scheme able to handle the new data rates. In addition, correction mechanisms for Single Event Upsets (SEU) and communication errors must be implemented to assure the integrity of the transmitted data. The L1DDC is a high speed aggregator board capable of communicating with multiple front-end (FE) electronic boards. It collects detector along with monitoring data and transmits them to a back-end system through bidirectional and/or unidirectional fibre links at 4.8 Gbps each. In addition, the L1DDC distributes synchronous clocks, trigger and configuration data coming from the back-end system to the FE boards. The L1DDC is completely transparent to the data being transmitted or received and can be used in any readout system. Three different types of L1DDC boards will be fabricated handling up to 9.6 Gbps of user data and consist of the same custom made radiation tolerant ASICs. The overall scheme of the data acquisition process and in particular the L1DDC board will be described. The results from the various system integration and radiation tests will be presented.

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