Hybrid GaN and CMOS integrated module radiation hard DC-DC converter

Ashwath Hegde[(1)], Yu Long[(2)], Alexander Odishvili[(2)], Esko Mikkola[(2)], Jennifer Kitchen[(1)], Ganeshprasad Gaonkar[(2)], Omkar Joshi[(2)], Dhruv Chaudhari[(2)], Gauri Koli[(1)], Pragya Malakar[(1)], Phaneendra Bikkina[(2)], Andrew Levy[(2)], Bertan Bakkaloglu[(1)]
[(1)]Arizona State University, [(2)]Alphacore, Inc.

Motivation

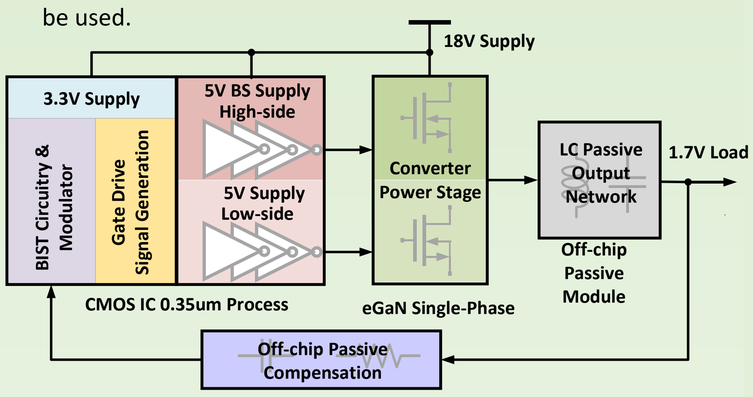
Develop reliable, low-mass, small-form factor, radiation-tolerant, high-performance, single-module point-of-load (POL) DC-DC buck converter(s) that support high energy physics (HEP) applications. It will not only be a good match to the power conversion system of the High Luminosity Large Hadron Collider (HL-LHC), but also has wide applications in future HEP experiments.

- Suitable for high radiation and magnetic field environments.
- Efficiently converts an input voltage of 10 - 18V to a regulated output of 1.2V - 5V with up to 10A load current.
- Realized within a small form factor for integration within the detector locations near the core.

Parameter	Specifications	Unit
Input Voltage	10 - 18	V
Output Voltage	1.2 - 5	V
Load Current	3 - 10	A
Overall Efficiency	70 - 80	%
Switching Speed	4 - 10	MHz
TID tolerance	200	Mrad
Neutron fluence (1 MeV eq.)	2E15	n/cm2
Air core inductor (min – max)	100 – 400	nH
Physical Dimensions (goal)	20 x 10 x 3	mm3

Design Innovations

- Highly integrated, high switching speed buck converter topology to achieve a small physical form-factor.
- Optimal division of functionality between Silicon and GaN to take advantage of inherent high current density and high switching speed of GaN devices for the crucial power stage and the versatility of CMOS to implement the bulk of the controller functionality .
- An enclosed layout transistor (ELT) technique and design flow to reduce the total ionized dose (TID) induced leakage[1].
- Innovative CMOS-based gate driver architectures that directly control the converter's high voltage GaN power stage by employing only thin gate-oxide low-voltage devices to maintain highest level of radiation hardness[2].
- On-chip high-efficiency voltage regulation and distribution schemes.
- Accurate on-chip Bandgap Reference (BGR) employing CMOS devices without radiation-prone bipolar devices[3]. Moreover, the on-chip BGR can be disconnected if an external voltage reference (such as a 130nm BGR chip) will be used.



Design Approach and Current Status

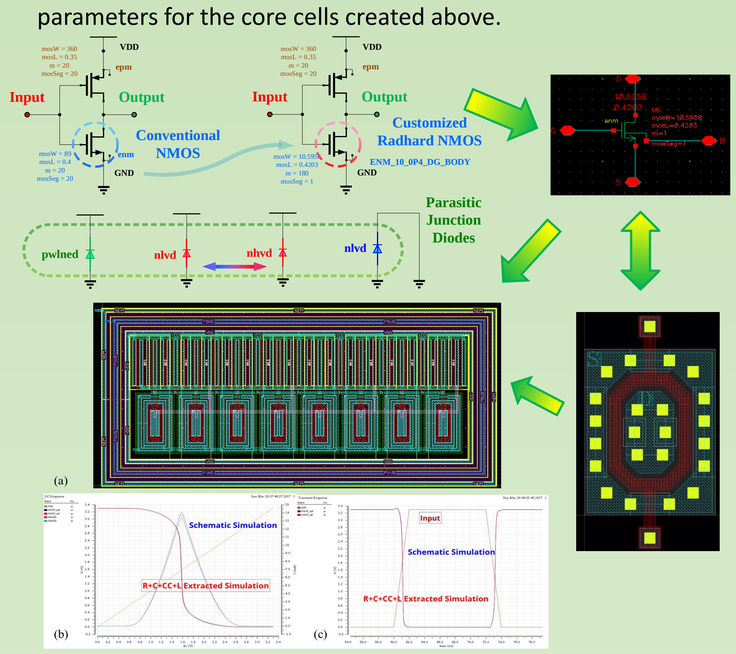
The design cycle up to this point has involved four steps.

- A printed circuit board (PCB) prototype design using discrete component-of-the-shelf (COTS) driver and controller IC's has been fabricated and tested in February 2017.
- A fully customized single-chip driver and controller IC enhanced with various RHBD techniques was taped out in a 0.35um CMOS process in July 2017.
- This CMOS chip was integrated into a hybrid GaN-CMOS converter module and tested in the spring of 2018. The module provides >70% efficiency in a 14V-to-1.5V conversion with 6A load current.
- "Final Version" of the controller chip will be taped out in September 2018. We have added protection schemes such as under-voltage lockout (UVLO), over-current protection (OCP), over-temperature protection (OTP), output voltage protection, adaptive dead-time control, etc.
- "Final Version" of the converter module will be tested in the spring 2019, including radiation tests.

Customized ELT NMOS P-cell Library

A fully customized ELT-type NMOS low-voltage core transistor library cells including different sizes of primitive cells (p-cell) based on the selected 0.35um CMOS process is developed to assist EDA design flow such as DRC, VLS and PEX process. The procedures can be divided into four steps.

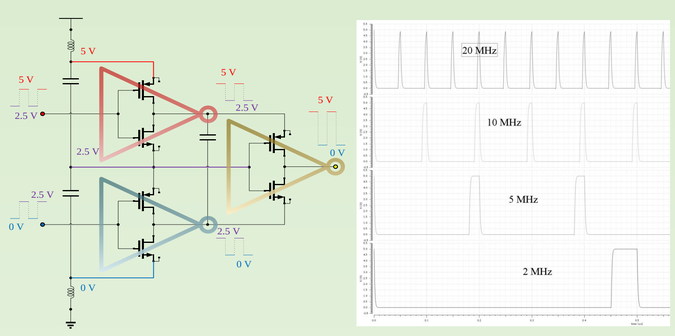
- Approximate a standard NMOS W, L and W/L with a Calibre extracted layout view.
- Create a complete DRC and LVS clean cell with all isolation ring, body contact and parasitic diodes added, run PEX simulation if necessary.
- Create/Update Cadence component description format (CDF) parameters for the core cells created above.



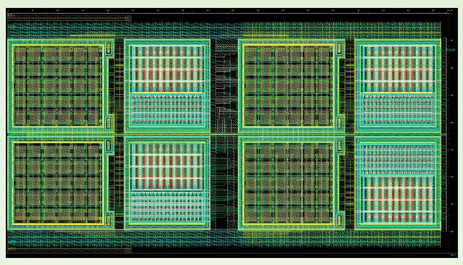
These illustrations above show the cell views of schematic, symbol and layout for a customized ELT NMOS.

Customized rad-hard IC Prototype

For maximum TID tolerance, 3.3V core MOSFET's are used to provide 5V gate driver output. A cascoded, or "house-of-card" structure is used to achieve the 5V output swing without exceeding the 3.3V V_{DS} break-down voltage[6] [7].



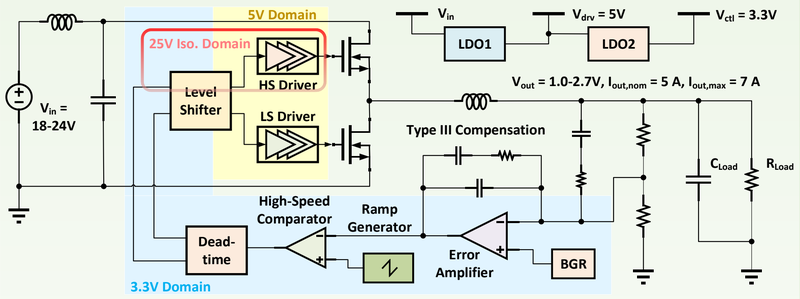
The high-side (HS) or low-side (LS) driver is shown in the figures. The schematic and its simulation waveforms at 2-20 MHz frequency with 20% duty-cycle validate the functions. The rad-hard layout with 25V isolation rings is shown below.

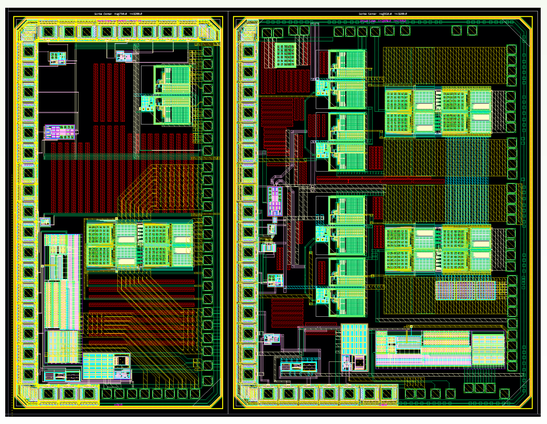


approx. size: 880 um x 440 um

Full Tape-out Schematic & Layout

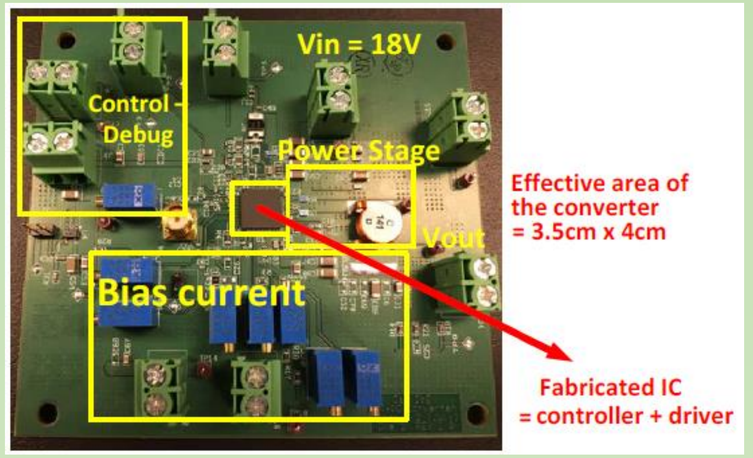
Figure below is the top-level diagram of the whole customized rad-hard driver and controller IC. The I/O LC filters and single-phase GaN power stage are off-chip.



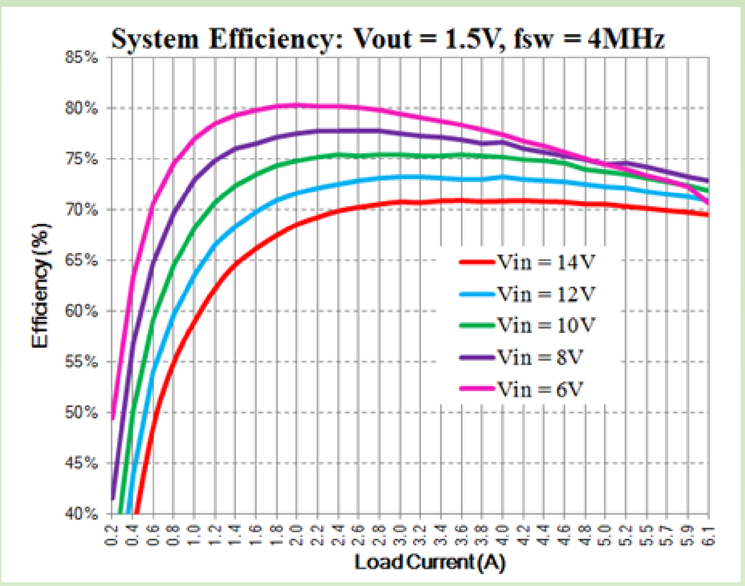


The chip on the left with a separate pad-frame contains individual blocks for testing, the larger pad-frame on the right is the full complete prototype IC fabricated in July 2017.

Test Results



Integrated CMOS IC + GaN power stage test module (size not optimized)



Evaluation results for the integrated CMOS IC + GaN power stage test module

Summary and Scheduled Future Work

- Highly integrated, high switching speed CMOS + GaN hybrid buck converter topology to achieve extreme radiation hardness and small physical form-factor is under development.
- A fully customized single-chip driver and controller IC enhanced with various RHBD techniques was taped out in a 0.35um CMOS process in July 2017.
- This CMOS chip was integrated into a hybrid GaN-CMOS converter module and tested in the spring of 2018. The module provides >70% efficiency in a 14V-to-1.5V conversion with 6A load current.
- "Final Version" of the controller chip will be taped out in September 2018. We have added features such as under-voltage lockout (UVLO), over-current protection (OCP), over-temperature protection (OTP), output voltage protection, adaptive dead-time control, etc.
- "Final Version" of the converter module will be tested in the spring 2019, including radiation tests.

References

[1] R. C. Lacoe, "Improving Integrated Circuit Performance Through the Application of Hardness-by-Design Methodology," *IEEE Transaction Nuclear Science*, vol. 55, no. 4, Aug. 2008, pp. 1903-1925.

[2] F. Faccio, G. Blanchot, et. al, "FEAST2: A radiation and magnetic field tolerant Point-of-Load buck DC-DC converter," *2014 IEEE Radiation Effects Data Workshop (REDW)*, Paris, France, Jul. 2014.

[3] J. Ramos-Martos, A. Arias-Drake, et al., "Evaluation of the AMS 0.35 um CMOS Technology for Use in Space Applications," the 4th International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications (AMICSA), Noordwijk, Netherlands, Aug. 2012.

[4] J. Wibben and R. Harjani, "A High-Efficiency DC–DC Converter Using 2 nH Integrated Inductors", *IEEE Journal of Solid State Circuits*, vol. 43, no. 4, pp.844-854, Apr. 2008.

[5] A. Hegde, Y. Long and J. Kitchen, "A Comparison of GaN-Based Power Stages for High-Switching Speed Medium-Power Converters," *the 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, USA, Nov. 2017.

[6] F. Neveu, B. Allard, C. Martin, P. Bevilacqua and F. Voiron "A 100 MHz 91.5% Peak Efficiency Integrated Buck Converter With a Three-MOSFET Cascode Bridge," IEEE Transactions on Power Electronics, vol. 31, no. 6, June 2016, pp.3985-3988.

[7] L. Salem, J. Buckwalter and P. Mercier, "A Recursive House-of-Cards Digital Power Amplifier Employing a λ/4-less Doherty Power Combiner in 65nm CMOS," in Proc. *of IEEE 42nd European Solid-State Circuits Conference (ESSCIRC) Conference*, Lausanne, Switzerland, Sep. 2016, pp. 189-192.

Acknowledgements

This work has been supported by the Department of Energy
Contract # DE-SC0015764

Contact

Esko Mikkola <esko.mikkola@alphacoreinc.com>