Hybrid GaN and CMOS integrated module radiation hard DC-DC converter

Develop reliable, low-cost, small-form factor, radiation-tolerant, high-performance, single-module point-of-load (POL) DC-DC buck converter(s) that support high energy physics (HEP) applications. It will not only be a good match to the power conversion system of the High Luminosity Large Hadron Collider (HL-LHC), but also has wide applications in other HEP experiments.

- Suitable for high radiation and magnetic field environments.
- Efficiently converts an input voltage of 10 - 18V to a regulated output of 1.2V - 5V with up to 10A load current.
- Realised within a small form factor for integration within the detector locations near the core.

### Design Innovations

- Highly integrated, high switching speed buck converter topology to achieve a small physical form-factor.
- Optimal division of functionality between SiC and GaN to take advantage of inherent high current density and high switching speed of GaN devices for the crucial power stage and the versatility of CMOS to implement the bulk of the controller functionality.
- An enclosed layout transistor (ELT) technique and design flow to reduce the total parasitic (TID) induced leakage.
- Innovative CMOS-based gate driver architectures that directly control the converter’s high voltage GaN power stage by employing only thin gate-oxide low-voltage devices to maintain highest level of radiation hardness.
- On-chip high-efficiency voltage regulation and distribution schemes.
- Accurate on-chip Bandgap Reference (BGR) employing CMOS devices without radiation-prone bipolar devices. Moreover, the on-chip BGR can be disconnected if an external voltage reference (such as a 130mV BGR chip) will be used.

### Design Approach and Current Status

The design cycle up to this point has involved four steps:

- A printed circuit board (PCB) prototype design using discrete component-off-the-shelf (COTS) drivers and controller IC has been fabricated and tested in February 2017.
- A fully customized single-chip driver and controller IC with enhanced RHBD techniques was taped out in a 0.35um CMOS process in July 2017.
- This CMOS chip was integrated into a hybrid GaN-CMOS converter module and tested in the spring of 2018. The module provides >70% efficiency in a 14V-to-1.5V conversion with 6A load current.
- “Final Version” of the controller chip will be taped out in September 2018. We have added protection schemes such as under-voltage-lockout (UVLO), over-current protection (OCP), over-temperature protection (OTP), output voltage protection, adaptive dead-time control, etc.
- “Final Version” of the converter module will be tested in the spring 2019, including radiation tests.

### Customized ELT NMOS P-cell Library

A fully customized ELT-type NMOS low-voltage core transistor library cells including different sizes of primitive cells (p-cell) based on the selected 0.15um CMOS process is developed to assistEDA design flow such as DRC, LVS and PEX process. The procedures can be divided into four steps:

- Approximate a standard NMOS W/L and W/L with a Calibre extracted layout view.
- Create a complete DRC and LVS clean cell with all isolation ring, body contact and parasitic devices added, run PEX simulation if necessary.
- Create/Update Cadence component description format (CDF) parameters for the core cells created above.

These illustrations above show the cell views of schematic, symbol and layout for a customized ELT NMOS.

### Design and Development

#### Circuit Topology

For maximum TID tolerance, 3.3V core MOSFETs are used to provide 5V gate driver output. A cascaded, or “house-of-card” structure is used to achieve the 5V output swing without exceeding the 3.3V Vds break-down voltage (1/2).

The high-side (HS) or low-side (LS) device is shown in the figures. The schematic and its simulation waveforms at 2.20 MHz frequency with 20% duty-cycle validate the functions. The rad-hard layout with 25V isolation rings is shown below.

Figure below is the top-level diagram of the whole customized rad-hard driver and controller IC. The I/O LC filters and single-phase GaN power stage are off-chip.

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### References


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