Remote Control and Calibration Module (BLERC) architecture

The figure shows the scheme of the firmware architecture, which is mainly divided into three functional blocks:

1. The diagnostic data streaming block is in charge of communicating with any kind of sensor or interface in order to collect system status information. This is a standardized module used in all the LHC injector BLM cards (called Diagnostic Reader). It contains as many interfaces submodules as required per card type. This module controls the readout intervals (which can be very different among the interfaces). Every readout is stored in a predefined package format and combined with the readout packages of the other interfaces. A scoreboard module monitors if every interface has updated its status since the last acquisition. The data are then written into a dual-port memory which is mapped into the memory space of the Nios II Soft-CPU.

2. The SoC, based on a Nios II Soft-CPU core working at 100MHz, is under control of a jCOS-II real-time operating system. The NIOS CPU is accompanied by a Triple Speed Ethernet (TSE) IP-core provided by Altera which implements the Gigabit Ethernet MAC communication and includes the 1000BASE-X/GSMDI Physical Coding Sublayer (PCS) logic with an embedded Physical Medium Attach (PMA). The TSE requires to work two Scatter-Gather Direct Memory Access (SGDMA) also provided by Altera. Three different on-chip memory modules have also been instantiated: one dual-port to store the diagnostic readout data, a second one to store the system descriptors used by the SGDMA modules. A software based TCP/IP Ethernet server is implemented and it periodically publishes the system status.

3. Finally a remote update functional block allows to remotely receive and upgrade the FPGA firmware and software as well as updates on default operational parameters.