Contribution ID: **143** Type: **Poster**

An automated pipeline for continuous integration of FPGA firmware and software for the LHCb Run3 upgrade

Tuesday, 18 September 2018 17:35 (15 minutes)

The readout system for the upcoming Run3 upgrade of the LHCb experiment at CERN is based on a common readout board called PCIe40. This common FPGA-based board can be reconfigured to serve different subsystems within LHCb. A CI/CD pipeline was implemented in order to automatically cross-validate the tight interaction between our custom FPGA firmware and the associated DAQ and control software, all being actively developed in parallel. We present challenges and solutions for applying this kind of practices, traditionally limited mainly to the field of software engineering, also to hardware-in-the-loop validation of FPGA firmware and SCADA-based control systems.

Summary

We present a CI/CD pipeline for cross-testing different components of the LHCb Run3 readout system. This automated flow simulates, synthesizes and finally validates on hardware the combination of our custom FPGA firmware, software and control system before their delivery to the rest of our scientific collaboration.

Primary author: DURANTE, Paolo (CERN)

Co-authors: GRANADO CARDOSO, Luis (CERN); VIANA BARBOSA, Joao Vitor (CERN); ALESSIO, Federico (CERN); VOUTERS, Guillaume (Centre National de la Recherche Scientifique (FR))

Presenter: DURANTE, Paolo (CERN)

Session Classification: Posters

Track Classification: Programmable Logic, Design Tools and Methods