Contribution ID: **134** Type: **Poster**

Machine learning: hit time finding with a neural network

Tuesday 18 September 2018 18:35 (15 minutes)

At the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan, the double-sided silicon strip sub-detector of the Belle II experiment is read out by 1748 APV25 chips.
FPGAs perform several calculations on the digitized signals. One of them is “Hit Time Finding”: the determination of the time and amplitude of the signal peaks of each event in real time using pre-programmed neural networks.
This work analyses the precision and reliability of these calculations depending of various parameters, the respectively required FPGA resources and the software for offline-learning of the node parameters using synthetic and pre-recorded data samples.

Summary

At the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan, the Belle II experiment will explore the asymmetry between matter and antimatter and search for new physics beyond the standard model.

One of its inner tracking systems is the Silicon Vertex Detector, which consists of 172 orthogonal double-sided strip sensors. They are arranged cylindrically in four layers around the Pixel Detector to measure the tracks of the collision products of electrons and positrons.
These sensors are read out by 1748 APV25 chips, one for 128 silicon strips, which output a time-multiplexed signal for each event and strip with a shaping time of about 50ns.
The analog data are then sent out of the radiation zone to 48 custom-built VME modules which convert them to digital, whereby 3 or 6 values per event of each strip are sampled at a frequency of 31.8 MHz.
FPGAs then compensate line signal distortions and reflections using digital finite impulse response filters and detect data frames from the incoming stream.
Then they perform pedestal subtraction, common mode correction and zero suppression, and finally “Hit Time Finding”: the determination of time and amplitude of the signal peaks of the clustered 3- or 6-sample APV25 outputs of each event in real time using pre-programmed neural networks.

This work analyses the precision and reliability of the calculations of the hit times and the amplitudes in dependence of different parameters like amount of neural nodes, neural layers, some selected activation functions, bits per interconnect-signals and calculation elements, signal shape and noise (artificial and real data) in connection with the respectively required resources (Gates, adders and multipliers in the DSPs, etc...) of the FPGA for optimization of the implementation in VHDL, as well as the software for offline-learning of the required node parameters and for the pre-calculation of the firmware performance using synthetic and pre-recorded data samples.
A comparison of the performance and the efficiency with the traditional method of using huge look-up-tables is also shown.

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Session Classification: Posters

Track Classification: Programmable Logic, Design Tools and Methods