A possible implementation of a detector specific extension of the FELIX firmware for the ATLAS ITk Pixel subdetector

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Introduction

In the course of the HL-LHC upgrade (2024-2026) with expected luminosities of up to $5 \cdot 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ ATLAS will perform the Phase-II upgrade. During this upgrade the complete Inner Detector of ATLAS will be replaced by the new **I**nner **T**rac**k**er (ITk).
ITk will consist of an outer strip-detector and an inner pixel-detector with both having completely new sets of front-end ASICs. While both sets allow the usage of the GBT protocol [2] on the downlink path, the ITk Pixel subdetector needs a different uplink protocol (i.e. the Aurora protocol [3]) due to the high data rates (up to 5.12 Gb/s per front-end) and the lpGBT chip not being radiation hard enough to be placed where it would be needed.
The new ATLAS-wide readout cards called FELIX (FrontEnd LInk eXchange) [4] will be used for translation between the front-end links and a COTS networking environment, in which all further processing steps are located. To fit the specific requirements of the ITk detector, this FELIX card needs some front-end specific firmware extensions.
This work shows a possible implementation of such a firmware extension for the ITk Pixel subdetector. It includes conversion of TTC signals into commands for the front-end chips as well as support for trigger tags instead of Bunch Crossing ID and Trigger ID for event identification for the downlink path. On the uplink side, an Aurora decoder block will be used for deserialisation and descrambling. Also, decoders and monitoring blocks are needed for low-level error handling and busy propagation.
This work can be beneficial for the ITk Strip subdetector as both subdetectors have some common features like 160 Mb/s downlink speed, 16 bit frame size and the usage of trigger tags.

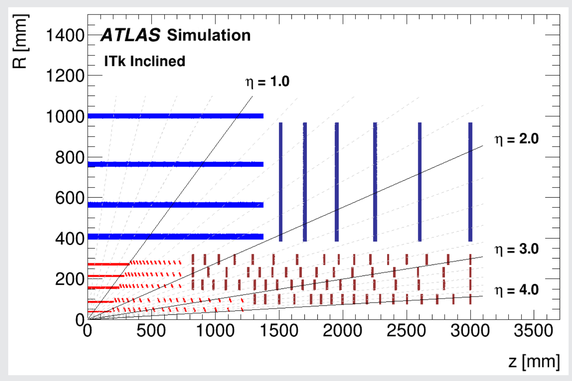

Figure 1: Possible ITk layout as presented in [1], with 13 space points up to $|\eta| \approx 4$ consisting of a pixel detector (red) and a silicon strip detector (blue).

Structure of the FELIX Firmware

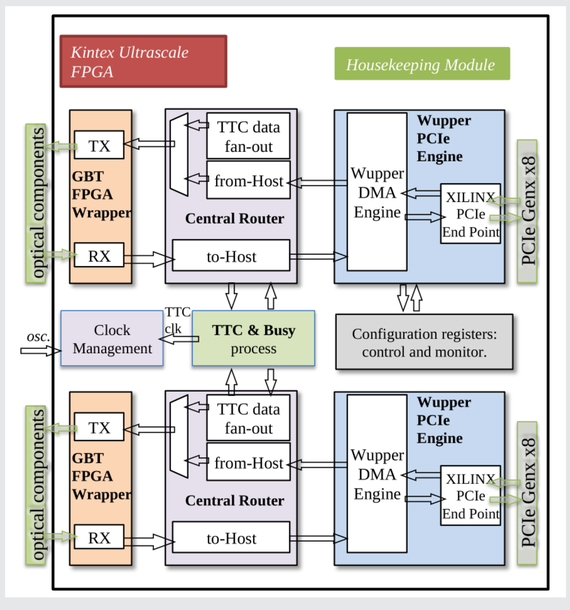

Figure 2: Block diagram of the Phase I FELIX firmware.

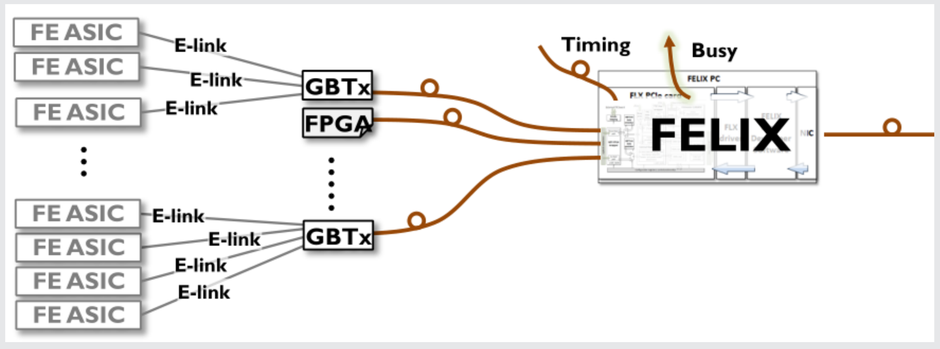

Figure 3: Overview on how GBT is used in connection with FELIX.

- Central Router is de-/multiplexing and en/-decoding the data to/from detector
- Uses so called ***E**(lectrical)-Link **Proc**essors*, short *EProcs*) for stream handling
- Each EProc is handling the up- or downlink of a single GBT E-Link
- FELIX card will be directly connected to the ITk detector with only optical-to-electrical conversion in between

⇒ Needs to encode data being sent to the detector and to decode the received data
⇒ Needs specialized EProcs for the ITk detector

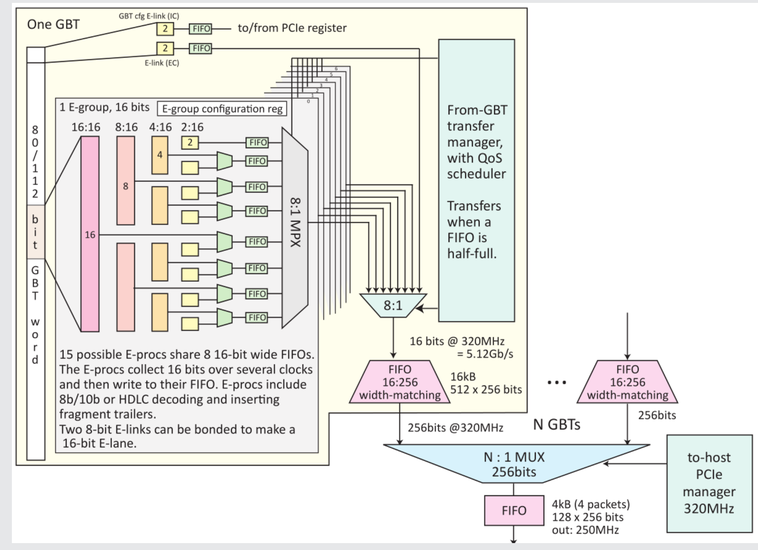

Figure 4: Detailed view of the uplink path within the Central Router. The downlink path is in principle the same with direction of the data flow being inverted.

Downlink path towards the detector

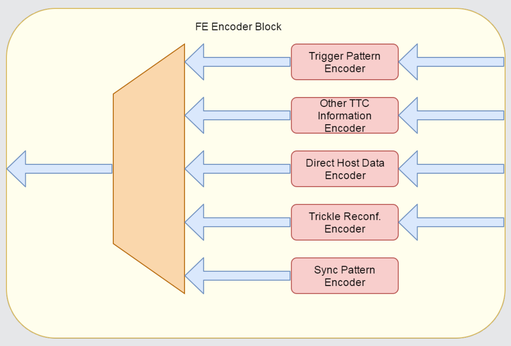

Figure 5: Block diagram for the modified downlink EProc for ITk Pixel. It combines data from several sources to be send to the detector.

- Data from several sources needs to be interleaved:
  - TTC signals from central trigger system
  - Commands coming from the readout SW
  - Continuous reconfiguration
  - *SYNC*/*IDLE* pattern to fill up empty slots
- Data is encoded in 16 bit frames, sorted by priority and send to the detector
- TTC frames can be sent at any time with no interference to read/write commands
- Allows to reconfigure the detector without pausing triggers

Uplink path from the detector

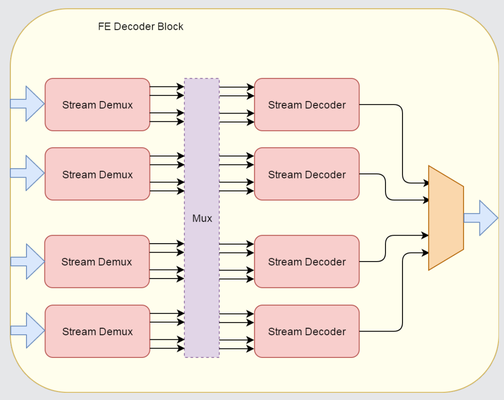

Figure 6: Block diagram for the modified uplink EProc for ITk Pixel. It decodes four optical links.

- Received stream consists of four logical streams and needs to be separated as these can come from different Front-End chips (FE chips)
- Necessary for decoding status signals and masking of disabled links
- *IDLE* frames will be thrown out to reduce the occupied bandwidth
- Optional multiplexer allows resorting of streams
- Filtered data is forwarded to the Routing Core and transmitted to the designated target

Update on Phase I FELIX firmware

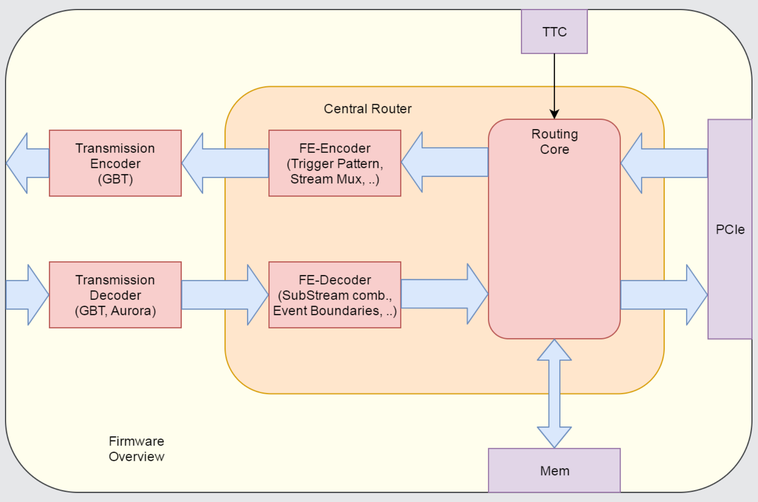

Figure 7: Block diagram of the modified Central Router.

- Also changes in the global firmware structure needed
- Need for memory to store the current configuration to be used for continuous reconfiguration
- Won't fit into the FPGA so an external memory is needed
- Two possible solutions for this:
  - Usage of the host system memory
  - Can be used with current FELIX cards which don't have external memory
  - But require additional bandwidth on the PCIe interface
  - External memory on the PCIe card
  - Adds the possibility to capture raw data in parallel to other operations for debugging

  ⇒ Would be very helpful for commissioning and testing new features

- Usage of so called *trigger tags* also needs adaptation
- Need to be generated in a deterministic way and replaced later in the processing path
- Several triggers can be grouped on the downlink and therefore have the same tag

⇒ This complicates tag handling as grouping depends on internal status of the FELIX FW

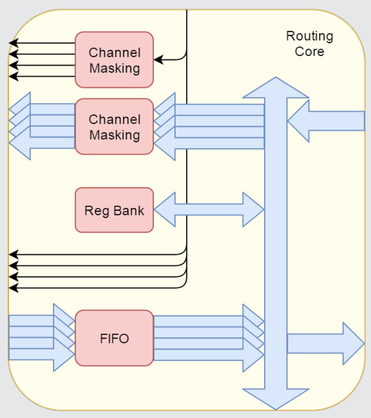

Figure 8: Block diagram of the additional features within the routing core.

References

[1] The ATLAS Collaboration, Technical Design Report for the ATLAS Inner Tracker Strip Detector, CERN-LHCC-2017-005 CERN (2017), https://cds.cern.ch/record/2257755.

[2] Moreira, P and Marchioro, A and Kloukinas, The GBT: A proposed architecure for multi-Gb/s data transmission in high energy physics, CERN-2007-007:332-336, https://cds.cern.ch/record/1091474.

[3] Xilinx, Aurora 64B/66B Protocol Specification https://www.xilinx.com/support/documentation/ip_documentation/aurora_64b66b_protocol_spec_sp011.pdf

[4] The ATLAS Collaboration, ATLAS Trigger and Data Acquisition Phase-II Upgrade Technical Design Report, ATL-COM-DAQ-2017-185 CERN (2017), https://cds.cern.ch/record/2296879/

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