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An Integrated SRAM Radiation Monitor in 180 nm CMOS Technology

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Introduction

In this research project, a custom SRAM (Static Random Access Memory) ASIC is developed. The device can act as a radiation monitor by measuring the number of Single-Event Upsets (SEUs) in ionizing environments. Many different measurement strategies exist to detect radiation, depending on its requirements such as total dose, energy spectrum or particle fluence. Examples include radfets and pixel chips which require sensitive analog readout circuits that may require calibration and can degrade at high dose levels. Many of these solutions are not monolithic and require a combination of different technologies. This approach can be implemented as a single-chip implementation and can support radiation monitoring applications with medium accuracy for mass scale deployments. The device was manufactured in a 180 nm CMOS technology.

Implementation

The memory contains 20 kbit 6T SRAM cells organized in 160 rows x 8 columns per bit and is read-out serially. All columns have a read/write circuit per bit. To measure radiation, the supply voltage of the memory is reduced to enhance the sensitivity of the SRAM cells since the Static Noise Margin is reduced. The content of the memory is periodically read and checked for upsets. During interfacing, the supply voltage is maximal to prevent erroneous operations. The interval with reduced supply voltage was 30s during the experiments and determines the probability of double bit flips. The SRAM core area of the prototype covers 700 µm x 700 µm and a reliable operation can be ensured down to 0.4 V.

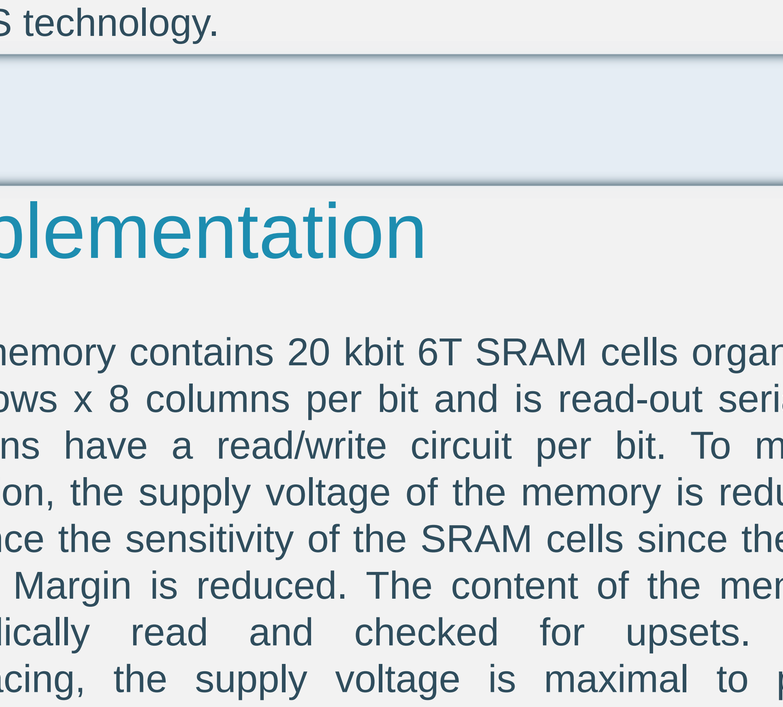

Figure 1

Results

The circuit was tested with heavy-ions (RADEF), protons (IRRAD), mixed particles (Charm) and a pulsed laser (KUL). Fig. 2a shows the laser scan results for reducing supply voltage of one bit with a 500 pJ pulse energy. The results show an increasing cross section with reducing supply voltage which is confirmed with heavy-ion experiments (Fig. 2b). More specifically, the multi-bit upset (MBU) cross section increases significantly. In Fig. 2c, the MBU/SEU ratio is plotted which shows a clear trend with LET at reduced supply voltage. This result is independent of the flux and proves that the device can estimate values of LET. The experiments also showed that this effect is data dependent.

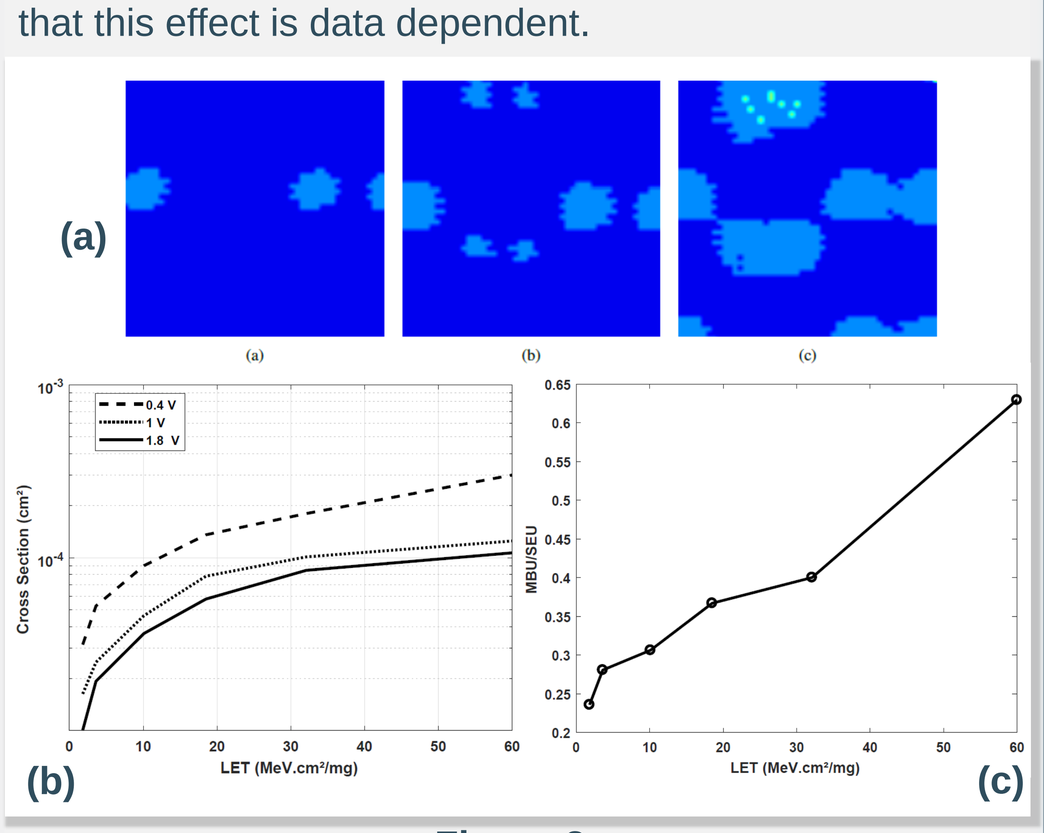

Figure 2

Conclusion

This work discussed radiation experiments with a 20 kbit custom SRAM memory in 180 nm CMOS technology. The sensitivity of the memory can be adjusted by reducing the supply voltage of the SRAM cells. Heavy-ion tests and pulsed laser experiments showed a significant dependency of the cross section on the supply voltage. Moreover, MBU analysis revealed a linear dependency on the LET.

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