Characterization of Soft Error Rate Against Memory Elements Spacing and Clock Skew in Logic with Triple Modular Redundancy in a 65nm Process

[1]Sandeep Miryala, [2]Tomasz Hemperek & [3]Mohsine Menouni

[1]Fermi National Accelerator Laboratory, [2]University of Bonn, [3]Centre de Physique des Particules de Marseille (CPPM)

Introduction

Single Event Effects (SEEs) in the form of Single Event Upsets (SEUs) and Single Event Transients (SETs) introduce soft errors in ASICs.

Triple Modular Redundancy (TMR) is a common practice to mitigate SEEs.

TMR is effective only if one of the memory element is affected by a particle strike. Hence, memory elements in a TMR must be spaced apart in the design layout.

SETs introduce unintended pulses and multiple circuits are designed to measure their width.

TMR with clock skew insertion mitigates SETs, such a test structures are designed.

A dedicated test chip (RD53SEU) is designed to study the soft error rates in a TMR logic and measure SET pulse width.

Triple Modular Redundancy Versions

a. TMR with out correction (Fig. 1a)
b. TMR with correction (Fig. 1b)
c. TMR with clock delay (Fig. 1c)

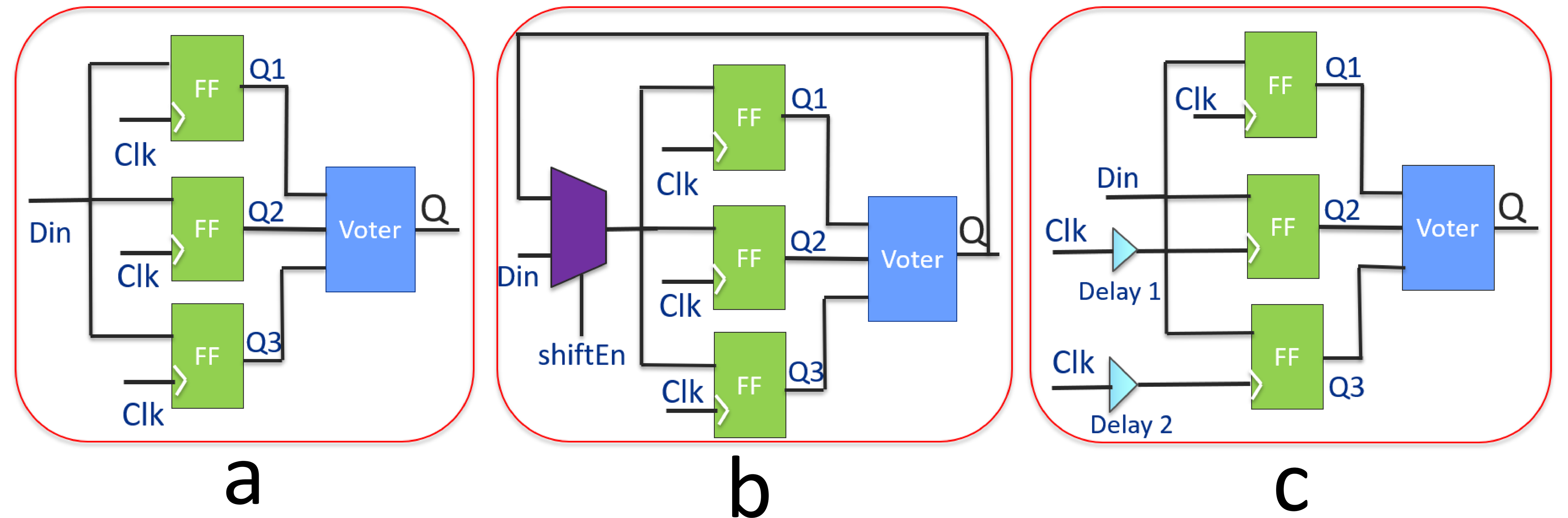


Figure 1. Triple Modular Redundancy versions implemented.

Shift Register Based Test Structures

Several shift register based test structures (Fig. 2) were designed on this chip with an objective to quantify the soft error rates on each of the TMR version. Table 1, summarizes the list of shift register based test structures.

The TMR memory element can be a latch or a flipflop. Different standard cells considered are DFQD, DFCNQD, LNQD, LNQD_Modified.

Each shift register is of 1kb size with serial input and output controlled by a shift enable signal.

Element spacing of 5uM, 10uM, 15uM is considered in a TMR.

Three different combinations of delay1 and delay2 are used for clock delay insertion version:

1. Delay1, Delay2 = 0.25ns, 0.50ns
2. Delay1, Delay2 = 0.5ns, 1ns
3. Delay1, Delay2 = 1ns, 2ns

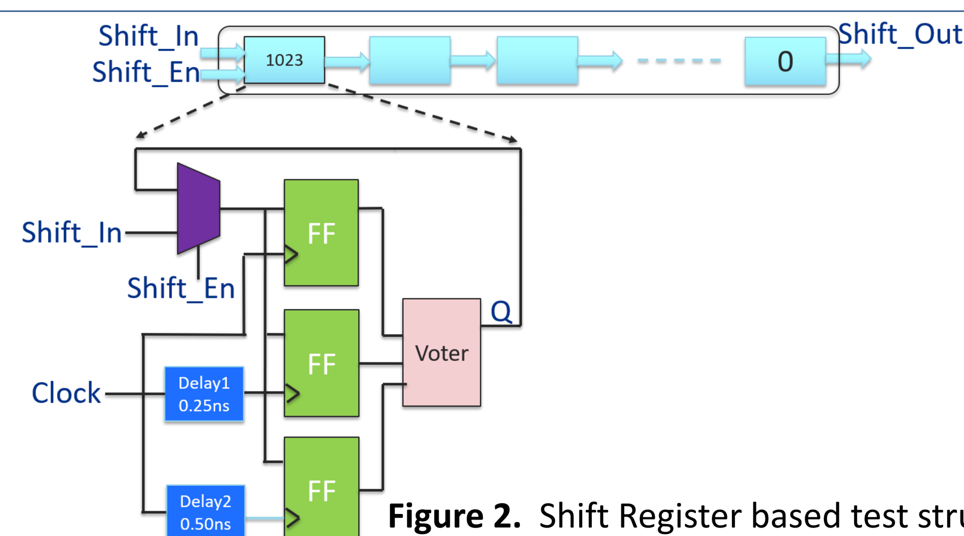


Figure 2. Shift Register based test structure

Table 1. List of shift register based f test structures

Test Structure #	Standard Cell	Description
1	DFQD1	No TMR
2	DFQD1	TMR with no element spacing
3	DFQD1	TMR with element spacing of 5uM
4	DFQD1	TMR with element spacing of 10uM
5	DFQD1	TMR with element spacing of 15uM
6	DFCNQD1	No TMR
7	DFCNQD1	TMR with no element spacing
8	DFCNQD1	TMR with element spacing of 5uM
9	DFCNQD1	TMR with element spacing of 10uM
10	DFCNQD1	TMR with element spacing of 15uM
11	LNQD1	No TMR
12	LNQD1	TMR with no element spacing
13	LNQD1	TMR with element spacing of 5uM
14	LNQD1	TMR with element spacing of 10uM
15	LNQD1	TMR with element spacing of 15uM
16	LNQD1 Modified	No TMR
17	LNQD1 Modified	TMR with no element spacing
18	LNQD1 Modified	TMR with element spacing of 10uM

Single Event Transient (SET) Measurement

Two different approaches to measure the pulse width and count the single event transients are designed. Both these approaches are based on a design containing two blocks:

a. SET target combinational logic block
b. SET analyzer block

Approach 1: Design based on the trigger capture: This test structure captures the SET pulse generated from the target block. The capture block composes of a series of inverter-latch combination. Each unit delay is ~40ps and the trigger is generated after 40th stage. This structure is more suitable for characterization of SET testing with a laser beam. This approach can be sensitive to SEU because of large number of latches and a flip-flop.

Approach 2: Design based on the temporal filtering: It consists of a target circuit and an analyzer circuit. The analyzer circuits is composed of a series of pulse filter flip-flops. The pulse filter is based on delay elements with different delay values.

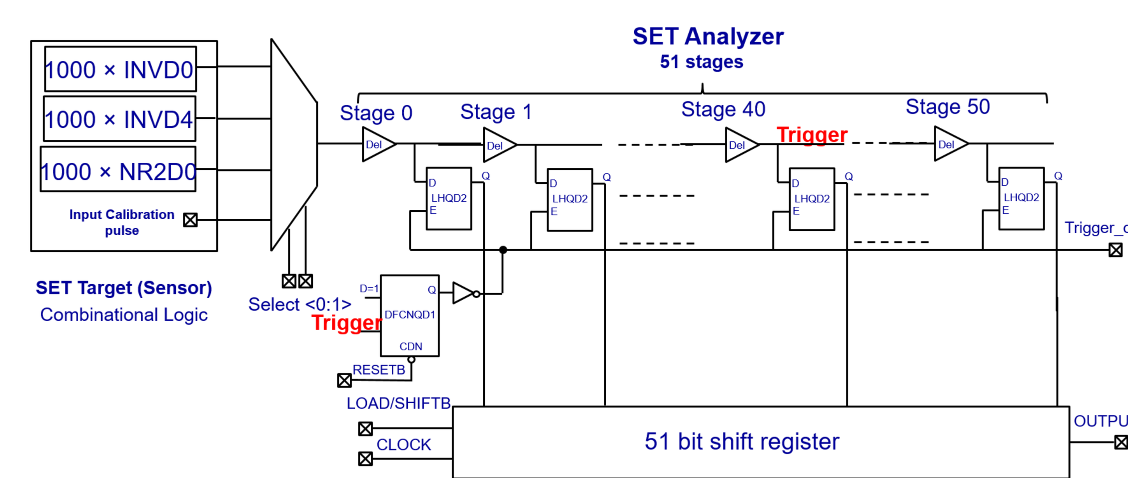


Figure 3. Approach 1: Design based on trigger capture

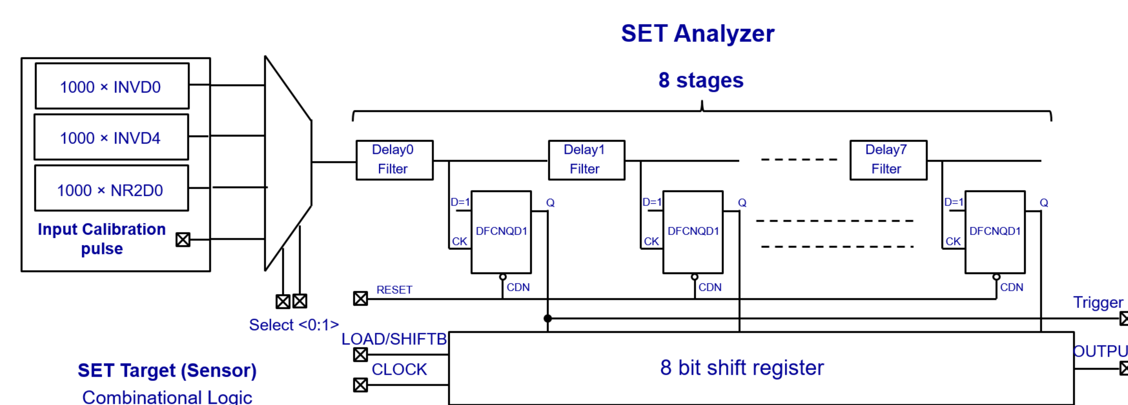


Figure 4. Approach 2: Design based on temporal filtering

	Del0	Del1	Del3	Del3	Del4	Del5	Del6	Del7
Delay	41 ps	86 ps	167 ps	257 ps	320 ps	410 ps	491 ps	648 ps

Power Integrity Analysis

Commercial industry standard tool is used for power integrity analysis. Static and Dynamic IR drop with VCD are carried out on the chip to make sure that the supply voltage is with in the acceptable range across the entire chip (Fig. 5 & Fig. 6).

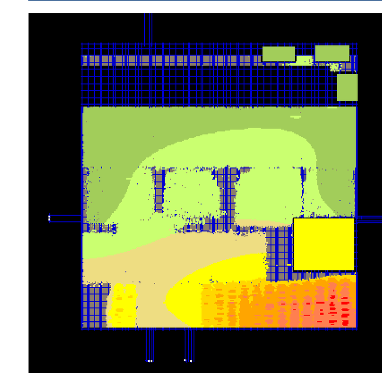


Figure 5. Static IR drop

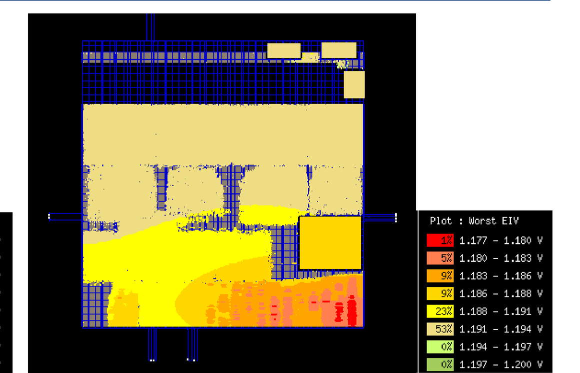


Figure 6. Dynamic IR drop

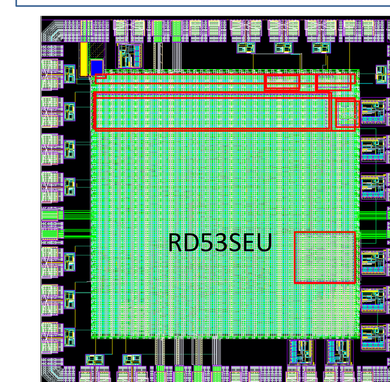
Implementation

TMR implementation is based on TMR based digital design flow (Fig. 7).

Functional verification with SDF back annotation.

Full chip spice simulation with parasitics.

- # of transistors : ~ 3.2 Million
- Simulation time : 1hr



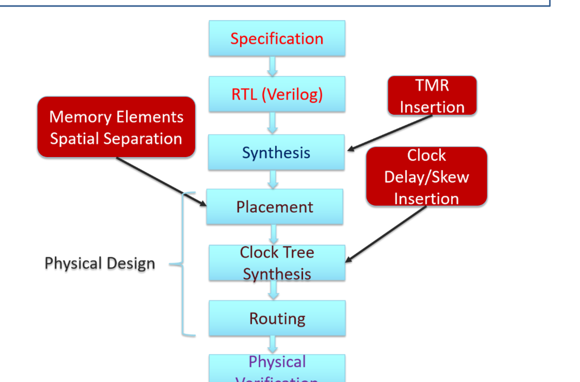


Figure 7. RD53SEU layout (left), TMR based digital flow (right)

Fabrication

The RD53SEU chip is a mini @SIC designed in 65nm process which is submitted for fabrication in Aug, 2018. The board design and test setup is underway.

Acknowledgements

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Project realized by:

Contact

Sandeep Miryala
Fermi National Accelerator Laboratory
Email: smiryala@fnal.gov
Website: http://ppd.fnal.gov/eed/eed_personnel.html
Phone: +1 630-840-2039

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