

Investigation of Single Event Latch-up effects in the ALICE SAMPA ASIC



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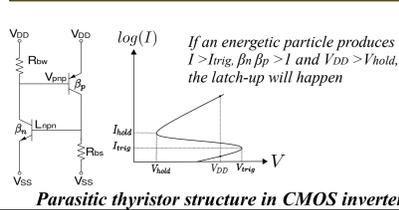
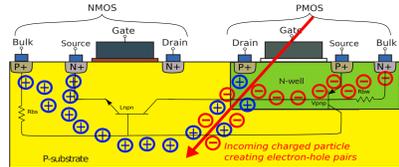
Introduction

Research Objective

During RUN 3 and RUN 4 at the Large Hadron Collider (LHC), the SAMPA chip is designed for the read-out front end electronics upgrade of the ALICE (A Large Ion Collider Experiment) Time Projection Chamber (TPC) and Muon Chambers (MCH). Previously, it was reported that the SAMPA V2 prototypes were susceptible to the high energy proton induced Single Event Latch-up (SEL) events. Further irradiation campaigns were required to find the source of SEL events in SAMPA V2 prototypes, and to verify that the SEL sensitivity of final versions (V3 and V4) of the SAMPA chip was reduced or even completely removed. The irradiation campaigns were performed using the Heavy-Ion facility at UCL (Université Catholique de Louvain - Belgique) and the Pulsed-Laser facility at IES (Institute of Electronics and Systems - Montpellier).

Single Event Latch-up

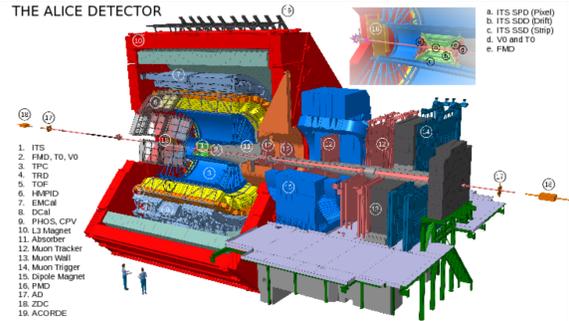
- Single Event Latch-up is caused by the passage of a single energetic particle through the sensitive regions of the device structure, resulting in the loss of device functionality.
- SEL triggers the parasitic thyristor structure in the CMOS (Complementary Metal-Oxide Semiconductor) device, forming a low impedance path between the power rails.
- This leads to an abnormal high-current state in the device and is typically corrected by power cycling the device.
- If SEL event is left uncorrected for a longer time period, the high-current path can cause melting and permanent damage to the device.



Parasitic thyristor structure in CMOS inverter

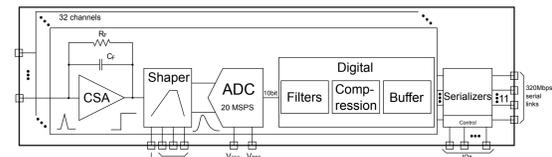
ALICE Experiment Upgrade for Run3 and Run4

- The ALICE experiment studies the particle production in heavy-ion (Pb-Pb), p-Pb and pp collisions at LHC, to characterize the strongly interacting matter at extreme energy densities where the Quark-Gluon Plasma (QGP) is produced.
- During Run3 and Run4, the expected interaction rate for the Pb-Pb collisions will be increased to 50 kHz.
- To cope with the higher interaction rates, a new front-end chip SAMPA was designed for the TPC and MCH detectors.



SAMPA Front-End chip

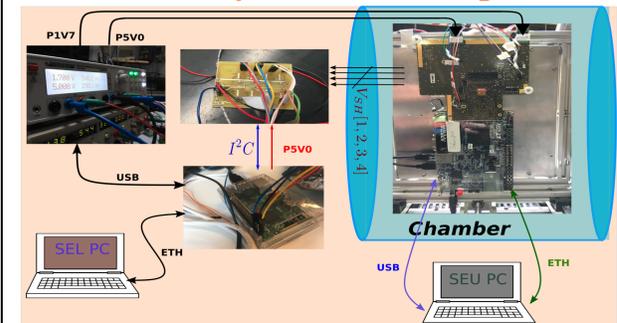
- The SAMPA chip is designed in TSMC 130 nm CMOS technology with a nominal supply voltage of 1.25 V.
- The SAMPA chip includes 32 data processing channels, each containing a charge-sensitive pre-amplifier, a shaper, a 10-bit 20 MHz Analog to Digital Converter (ADC) followed by a Digital Signal Processor (DSP).
- The data are read out, either in continuous or triggered mode, through eleven 320 Mbps SLVS serial links.
- The SAMPA chip should withstand :
 - Total Ionizing Dose (TID) of 2.1 kRad, and
 - a flux of 3.4 kHz/cm² of High Energy Hadrons (HEH).



Block diagram of SAMPA chip

SAMPA V2 Heavy-Ion SEL campaign

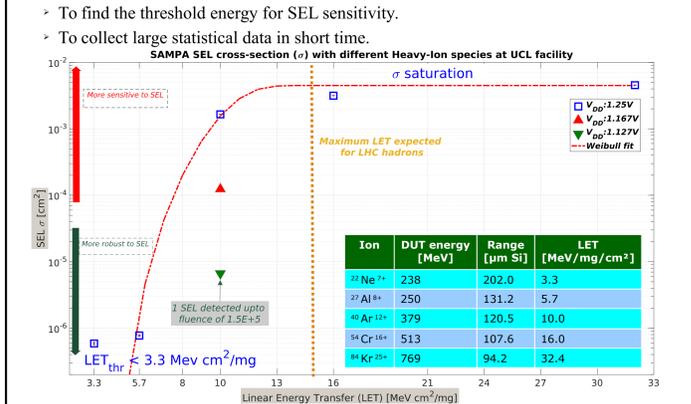
SAMPA Heavy-Ion Test-setup



- SAMPA carrier board (DUT) and FPGA DAQ board are placed inside the vacuum chamber and are connected together via HSMC connector.
- Programmable power supply (HMP2020) provides 2 supply voltages to the DUT through BNC connectors. In addition, special cables are prepared to power on the FPGA DAQ board.
- Current monitoring board measures voltage drops on DUT's power domains via BNC connectors and sends the data to Raspberry Pi.
- Raspberry Pi receives data from the power supply and current monitoring board and transmits the data to SEL PC via Ethernet cable.
- DUT power cycles automatically if the current consumption exceeds certain threshold (SEL).

Why Heavy-Ion campaign ?

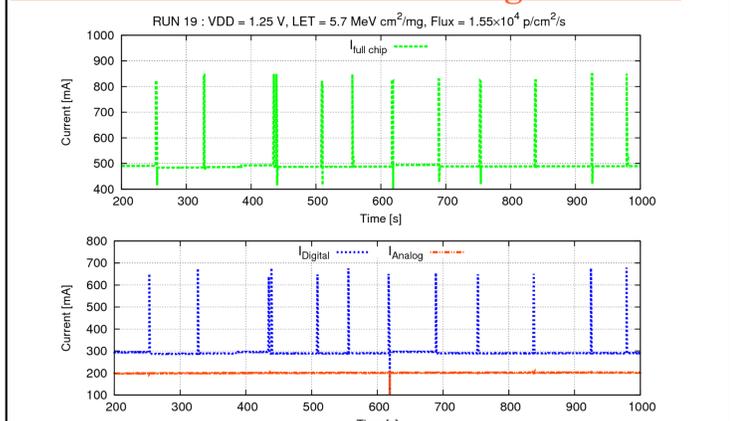
- Heavy-Ion irradiation campaign offers a complete characterization of the SEL sensitivity of the SAMPA V2 prototypes. It allows :
 - To find the threshold energy for SEL sensitivity.
 - To collect large statistical data in short time.



Ion	DUT energy [MeV]	Range [μm Si]	LET [MeV/mg/cm ²]
²² Ne ⁺⁺	238	202.0	3.3
²⁷ Al ⁺⁺	250	131.2	5.7
⁴⁰ Ar ⁺⁺	379	120.5	10.0
⁵⁴ Cr ⁺⁺	513	107.6	16.0
⁸⁴ Kr ⁺⁺	769	94.2	32.4

- Heavy-Ion results demonstrate that SEL σ curve saturates above LET of 10 MeV cm²/mg and falls off rapidly between LET of 5.7 and 10 MeV cm²/mg.
- The reduction of supply voltage confirmed correlation with the SEL sensitivity.
 - The nominal supply voltage is larger than the hold voltage of the parasitic thyristor structure.

First evidence towards the origin of SEL

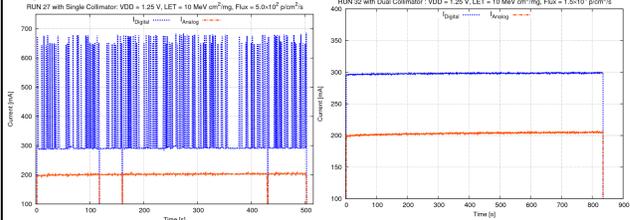
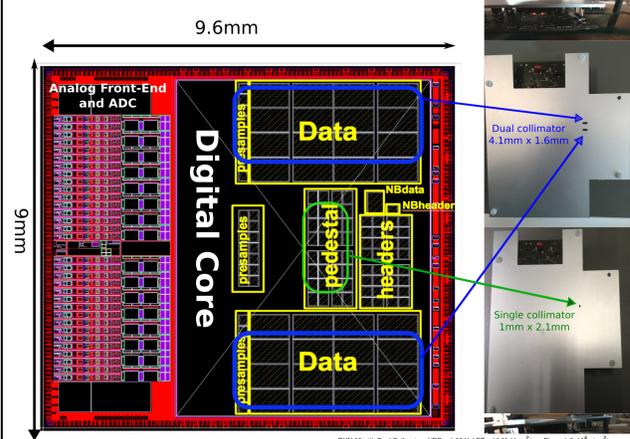


- Heavy-Ion tests indicate SEL events only in the digital power domain. The spikes in the digital current domain were correlated with the burst of Single Events Upsets observed in the pedestal SRAM (Static Random Access Memory) IPs.
 - Pedestal SRAM IPs were single port compared with other SRAM IPs (dual port) in V2.
- Detailed layout verification was performed on both SRAM IPs.
 - Single port memory substrate/well contacts density is lower than dual port memory.

Experimental methods to localize the origin of SEL in V2 Digital core

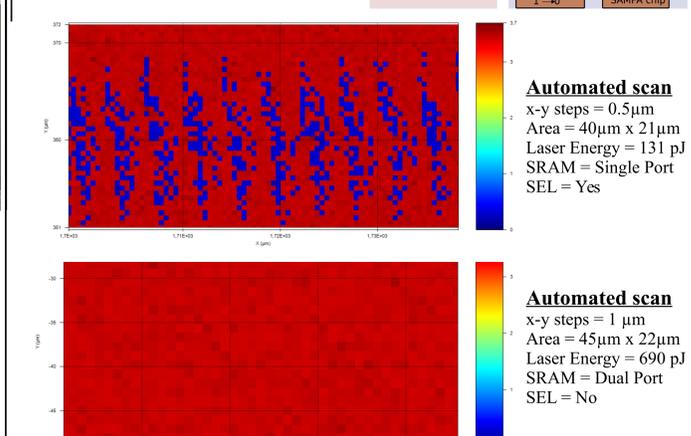
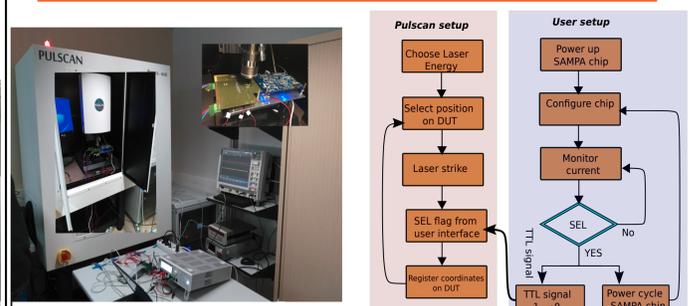
1. Heavy-Ion tests with collimators

- Developed 2 aluminum collimators with thickness of 2 mm.
 1. Dual collimator to irradiate SAMPA dual port SRAM IPs
 2. Single collimator to irradiate only SAMPA single port SRAM IPs



A lot of current spikes were detected on digital power domain using single collimator. At same LET value, no current spike was detected using dual collimator.

2. Backside irradiation with Pulsed-Laser



SEL mitigation in SAMPA V3 and V4

SAMPA V3 and V4 SEL tests

- Pedestal SRAM IPs are modified from single port to dual port in final versions of the SAMPA chip.
 - The irradiation campaigns approved that dual port SRAM IPs are robust against SEL effects.
 - From radiation perspective, the functionality of SAMPA V3 and V4 prototype is identical.
- Another Heavy-Ion campaign was conducted in November 2017 to evaluate the sensitivity of SAMPA V3 and V4 against SEL events.
 - No SEL event is detected in any of the irradiated samples.
 - One V4 sample tested at different LET values up to 125 [MeV cm²/mg] (45°C).
 - One V3 sample tested at maximum LET value of 125 [MeV cm²/mg] (60°C).
 - Another V4 sample tested at maximum LET value of 125 [MeV cm²/mg] (85°C).
- During Pulsed-Laser campaign, an automated scan was performed on the same pedestal memory region in SAMPA V4 sample.
 - No SEL event was detected up to 1025 pJ of laser energy.

Conclusions

- Heavy-Ion campaign indicated that SAMPA V2 prototypes were highly sensitive to SEL events.
 - SEL LET_{thr} < 3.3 MeV cm²/mg makes it critical to operate safely in the ALICE radiation environment.
- Both Heavy-Ion and Pulsed-Laser campaigns verified that the cause of SEL events was related to single port SRAM IPs in the V2 prototypes.
 - Due to the larger distance between the n-well and substrate contacts to the P+ and N+ implants of the CMOS circuits.
 - Pulsed-Laser automated scan showed that the SEL events trigger only inside the bit-cell circuits of the single port SRAM IP, and not in the periphery circuits.
- The campaigns confirmed that SAMPA SEL sensitivity reduced linearly by decreasing the supply voltage and completely removed below 1.1 V.
- The campaigns assured that the final versions V3 and V4 of the SAMPA chip are unsusceptible against SEL effects and fully qualify to operate in the ALICE radiation environment.

Acknowledgements

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