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A Delay Locked Loop for Time-to-Digital Convertors with Quick Recovery and Low Hysteresis

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1. Abstract

In this paper a Delay Locked Loop (DLL) is designed in 65nm CMOS Technology. The benefits of this DLL is the Quick recovery from an out-of-lock state and a lower in lock hysteresis due to an new type of Bang-Bang phase detector (BBPD). The quick recovery is accomplished using two BBPD's which both operate in a different region, controlled by a 3-state controller. Both PD's are of the bang-bang type because it can more easily be triplicated for an increased radiation tolerance.

2. Implementation

The Phase detector in this design has two features: (1) Fast recovery, which is accomplished by the 3-state controller and (2) low hysteresis. The first feature is a result of the 3-state controller which detects 4 different phases of the delay line, a very early or very late state which is fed to a strong charge pump and a regular early and late state which is sent to a weak charge-pump. The early/late detection is detected by the new type of PD shown in figure 1.

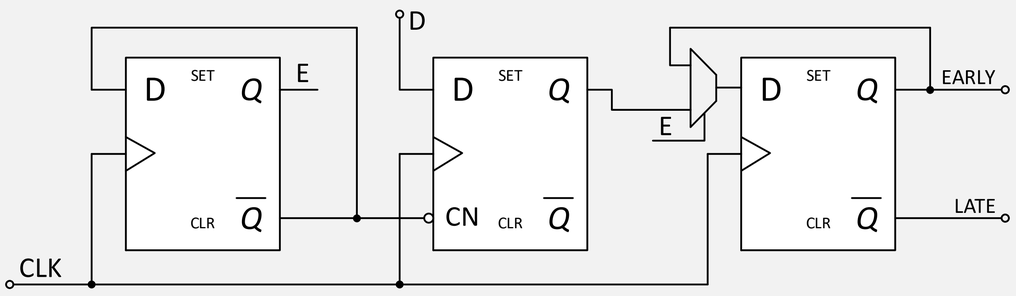

Figure 1

This phase detector addresses the problem of a sticky output of the phase detector results in hysteresis. This issue is improved by placing a reset period before every phase detecting period. In this way, every phase detection starts from the same output state. A typical timing diagram of this phase detector is shown in Figure 2. By using this technique, the phase detection hysteresis is reduced but also the detection speed is divided by 2. This, however, results in a more stable limit cycle of the DLL, resulting in a decreased output jitter. As shown in Figure 3, simulations show that the benefits of having a lower hysteresis, outweigh the lower phase detection speed. The blue graph shows the variation of the in-lock delay when using a traditional BB phase detector, which has high hysteresis. The red graph shows the delay when using the improved phase detector. Comparing the two, the proposed phase detector results in a delay variation which is 40 times smaller compared to the traditional phase detector.

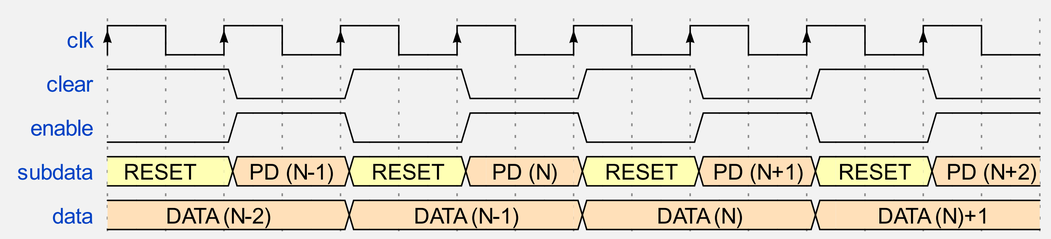

Figure 2

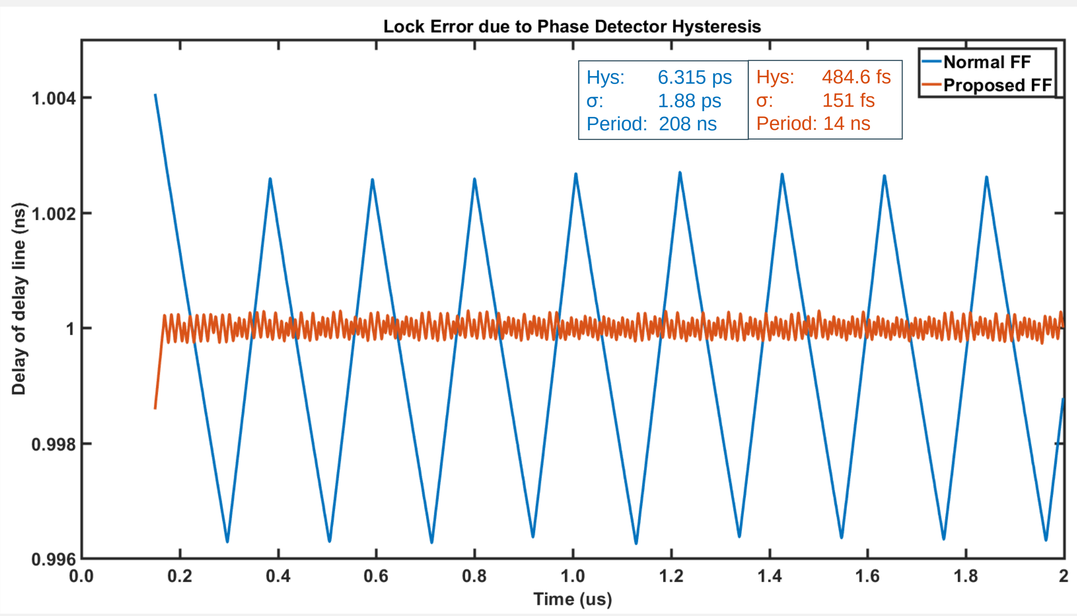

Figure 3

Figure 4 shows a complete lock cycle when the loop starts completely out of lock. Notice the fast recovery region and the slower region. This is due to the two charge pumps which are controlled by the 3-state controller. The total lock cycle takes less than 1 µs to get back into a locked state.

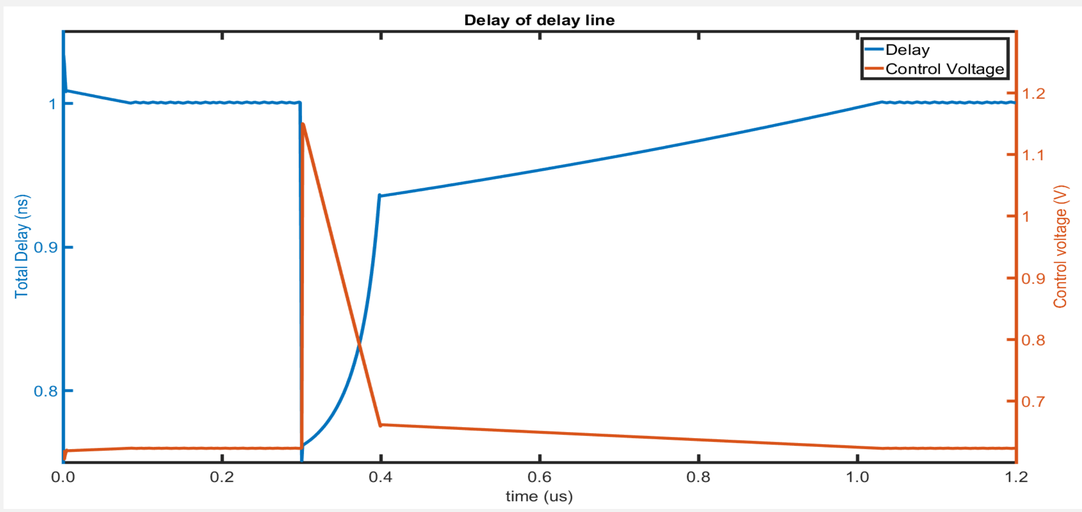

Figure 4

3. Conclusion

Techniques to improve acquisition time as limit cycle jitter have been demonstrated. Both improvements, a novel phase detector with four levels and a bang-bang PD with low hysteresis, enable an extremely fast recovery time below 1 µs in combination with a simulated loop hysteresis of 400 fs. Combining these two techniques can be useful in applications such as a full DLL based TDC,