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Delay Locked Loop for use in a time-to-digital converter with quick recovery and low hysteresis

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This paper proposes a 1 GHz Delay Locked Loop (DLL) which was processed in a 65 nm CMOS technology. The circuit was designed for harsh environments, in particular ionizing radiation. It has a single event recovery time of less than 1 us. The DLL is used inside a Time to digital converter (TDC), and achieves an rms jitter below 800 fs. One of the improvements to this low jitter comes from the bang-bang phase detector (PD), which is designed to have a very small hysteresis of only 480 fs.

Summary

Nowadays a lot of applications need a very accurate time representation for time-domain signal processing. Examples are the large number of particle detectors in high energy physics experiments like ATLAS and CMS at the Large Hadron Collider (LHC) in CERN, but also applications like Time of Flight (TOF) and LIDAR measurements. Inside these applications the valuable information can be found inside the timing differences between signals. This timing difference is then converted to a binary representations, using a time to digital converter (TDC).

The performance of a DLL will contribute to the quality of the TDC. In this paper the focus is on the fast recovery form single event effects, and the low hysteresis of the bang-bang phase detector. Due to the nature of the architecture of the DLL, PVT (Process Voltage Temperature) variations and TID (Total Ionizing Dose) effects are compensated. The DLL is composed of 128 delay stages which lead to a timing bin size of 7.815 ps.

The fast recovery of the DLL is accomplished by use of a multiphase PD, which can detect four different states: very-early, early, late and very-late. The very-early and late detections are generated by delaying either the reference signal or the DLL. These outputs are then sent to a charge pump designed for a larger current of 100 uA to charge and discharge the loop filter. This last circuit is also triplicated because a misfire of the very-early and late PD can lead to large changes in the delay line. The early-late detection in the multiphase PD is based on a bang-bang phase detector. A common problem with bang-bang PD's is the hysteresis which leads to larger jitter. The hysteresis problem, in a bang-bang PD based on a D-flipflop (DFF), is due to the fact that the output state has an influence on the decision voltage of the input of the DFF, similar to a memory effect. In this design this problem is overcome to operate the PD in two stages. Where the first stage will always be reset to the same starting-state to reduce the memory effect, in a second stage the actual phase detection is made. The output of this bang-bang PD is connected to a charge pump, which is designed to deliver a smaller current that operates after settling. This lower current and the low hysteresis PD helps in decreasing the jitter of the DLL feedback system. In order to increase the robustness against single event transients (SET), the loop filter of the charge pump is enlarged such that the control voltage of the delay line will only be affected slightly when an SEE occurs at this node.

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