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ATLAS Tile Calorimeter Link Daughter Board

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Summary

We have developed an updated DaughterBoard design for control and readout of the upgraded ATLAS hadronic Tile Calorimeter electronics for HL-LHC. The new design migrated from two QSFPs to four SFP+ modules handling: 4×9.6 Gbps uplinks operated by two Kintex Ultrascale+ FPGAs, and 2×4.8 Gbps downlinks operated by two GBTxs. The uplink sends continuous high-speed readout of digitized PMT samples, while the downlink receives control, configuration and LHC timing. TMR, FEC and CRC strategies, plus a double redundant design with radiation tolerant components, minimize single failure points and improves resistance to single-event upsets caused by minimum ionizing and hadronic radiation.

This talk will describe the architecture, radiation and beam tests of versions 3 and 4, and design of the current version 5 board.

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