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GSPS: a 1 GS/s sampling digitiser designed with interleaved architecture for the LaBr3 detectors of the FAMU experiments.

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A fast continuously sampling digitiser have been designed for acquiring the signal from LaBr3 scintillating crystals detectors. They are foreseen in the FAMU experiment, aimed at spectroscopic measurements of muonic hydrogen, possibly providing insights into proton radius puzzle. The board, named GSPS, is an FMC mezzanine which hosts two off-the-shelf sampling ADC used in interleaved timing architecture, achieving 1 GS/s rate. Interleaved technique allows us to keep both lower production costs and simple acquisition system avoiding complex interface protocols like JESD204. The board will be described, tests and achieved performances will be shown and discussed.

Summary

The GSPS board is a project developed for the FAMU experiment aimed at performing a spectroscopic measurement of the hyperfine transition of the 1S state of muonic hydrogen, possibly getting new evidences on proton structure and possibly providing insights into proton radius puzzle. The Bologna Division of I.N.F.N. and the Physics Department of the University of Bologna are developing X-rays detectors to achieve good timing and energy resolution, made with Lanthanum bromide scintillating crystals [LaBr3(Ce)] coupled with a high quantum efficiency photomultiplier. Fast sampling electronics must to be designed in order to acquire a number of samples during the rising edge of the signal which are sufficient for exploiting the detector performances in terms of energy and timing resolution. The first prototype, named GSPS, is an FMC mezzanine which hosts two off-the-shelf sampling ADC from Analog Device (12-bit, 500 MS/s) used in interleaved timing architecture so that the target of 1 GS/s can be achieved. The interleaved technique has been chosen to discard ADCs with JESD204 output interface and, consequently, keeping simpler requirements for the acquisition part which is implemented on FPGA. The GSPS board will be described, discussing the main solutions adopted both for analog and digital part; besides, relevant design and technological aspects will be shown as well.

As for the acquisition system, it has been achieved by plugging the GPSP mezzanine onto a commercial board called ZedBoard, hosting a Xilinx Zynq FPGA. A custom firmware core has been designed to continuously acquire samples from the GSPS; after being triggered (from external signal or by the ADC data themselves) a software running over the ARM processor embedded in the Zynq FPGA send the buffer through TCP/IP to a custom program running on a PC devoted both to data recording on disk and on-line monitoring using MATLAB digital signal processing functions. The GSPS has been thoroughly tested both for static and dynamic performance: the setup will be presented. Performances will be presented: mainly signal-to-noise ratio, gain, offset, harmonic distortion (THD, SINAD, ENOB) and non-linearities (INL,DNL). All measurements have been repeated for each ADC and for the interleaved system as well. Effect on interleaved performance due to mismatches will be pointed out. Mitigation techniques as the filtering with fractional delay filters will be discussed showing as they have been applied to get an ENOB = ˜ 9. A new board revision in currently under design to be tested for the FAMU data taking campaign foreseen at the end of 2018 at the Rutherford and Appleton Laboratory in U.K. Status and highlights of the new design will be presented.

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